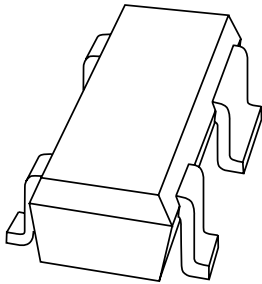


# DATA SHEET



## **BFG480W** NPN wideband transistor

Product specification  
Supersedes data of 1998 Jul 09

1998 Oct 21

## NPN wideband transistor

## BFG480W

## FEATURES

- High power gain
- High efficiency
- Low noise figure
- High transition frequency
- Emitter is thermal lead
- Low feedback capacitance
- Linear and non-linear operation.

## APPLICATIONS

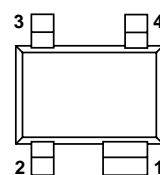
- RF front end with high linearity system demands (CDMA)
- Common emitter class AB driver.

## DESCRIPTION

NPN double polysilicon wideband transistor with buried layer for low voltage applications in a 4-pin dual-emitter SOT343R plastic package.

## PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	emitter
4	collector



Top view MSB842

Marking code: P6.

Fig.1 Simplified outline SOT343R.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{CE0}$	collector-emitter voltage	open base	–	4.5	V
$I_C$	collector current (DC)		80	250	mA
$P_{tot}$	total power dissipation	$T_s \leq 60\text{ }^\circ\text{C}$	–	360	mW
$f_T$	transition frequency	$I_C = 80\text{ mA}$ ; $V_{CE} = 2\text{ V}$ ; $f = 2\text{ GHz}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	21	–	GHz
$G_{max}$	maximum gain	$I_C = 80\text{ mA}$ ; $V_{CE} = 2\text{ V}$ ; $f = 2\text{ GHz}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$	16	–	dB
F	noise figure	$I_C = 8\text{ mA}$ ; $V_{CE} = 2\text{ V}$ ; $f = 2\text{ GHz}$ ; $\Gamma_S = \Gamma_{opt}$	1.8	–	dB
$G_p$	power gain	Pulsed; class-AB; $\delta < 1 : 2$ ; $t_p = 5\text{ ms}$ ; $V_{CE} = 3.6\text{ V}$ ; $f = 2\text{ GHz}$ ; $P_L = 100\text{ mW}$	13.5	–	dB
$\eta_C$	collector efficiency	Pulsed; class-AB; $\delta < 1 : 2$ ; $t_p = 5\text{ ms}$ ; $V_{CE} = 3.6\text{ V}$ ; $f = 2\text{ GHz}$ ; $P_L = 100\text{ mW}$	45	–	%

## CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

NPN wideband transistor

BFG480W

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

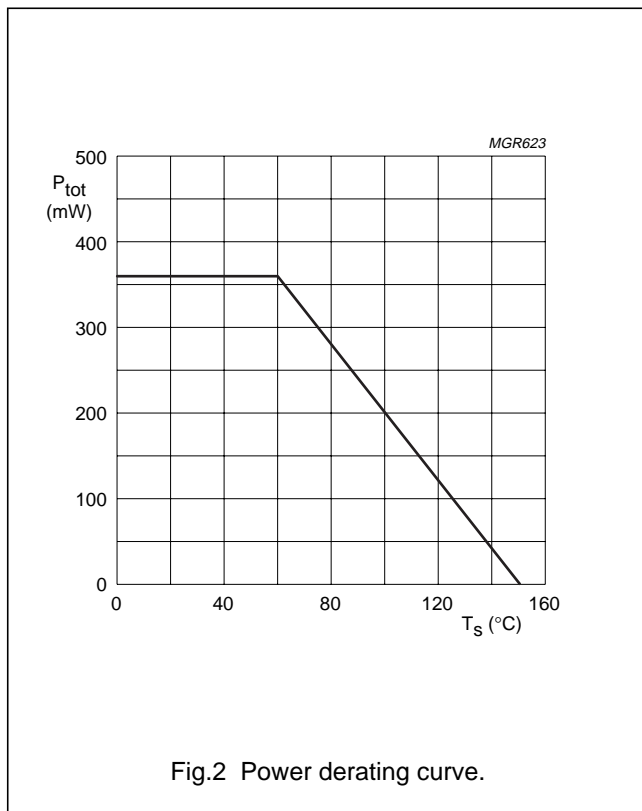
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	14.5	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	4.5	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	1	V
I <sub>C</sub>	collector current (DC)		–	250	mA
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> ≤ 60 °C; note 1; see Fig.2	–	360	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	operating junction temperature		–	150	°C

**Note**

1. T<sub>s</sub> is the temperature at the soldering point of the emitter pins.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-s</sub>	thermal resistance from junction to soldering point	250	K/W



## NPN wideband transistor

## BFG480W

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

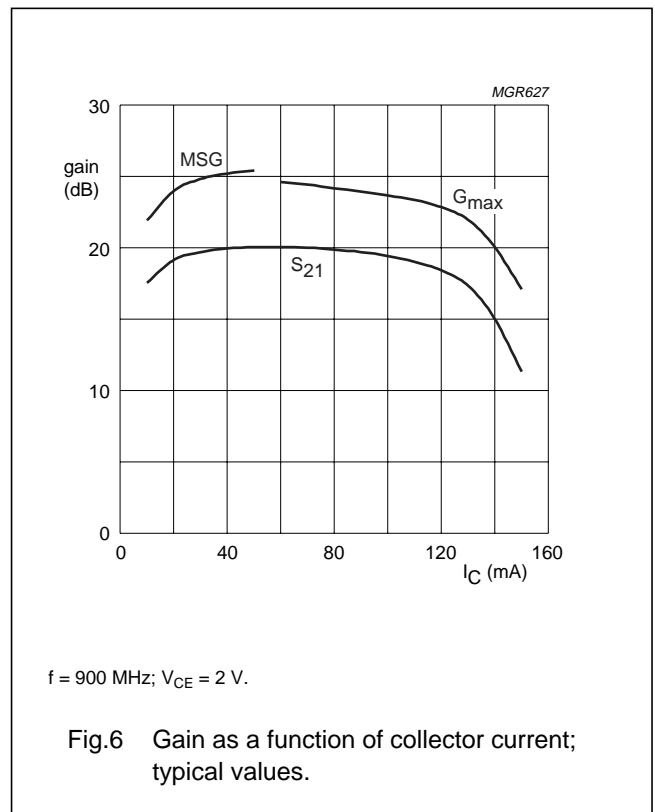
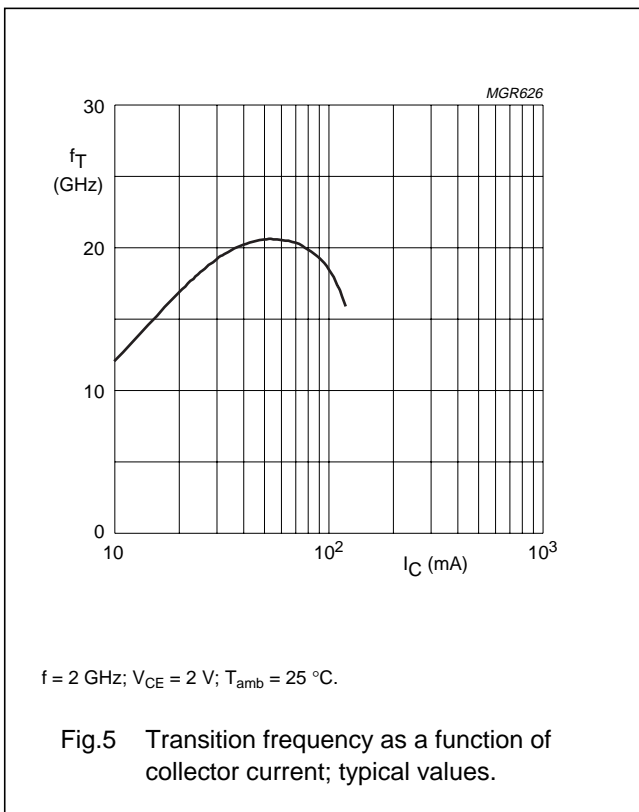
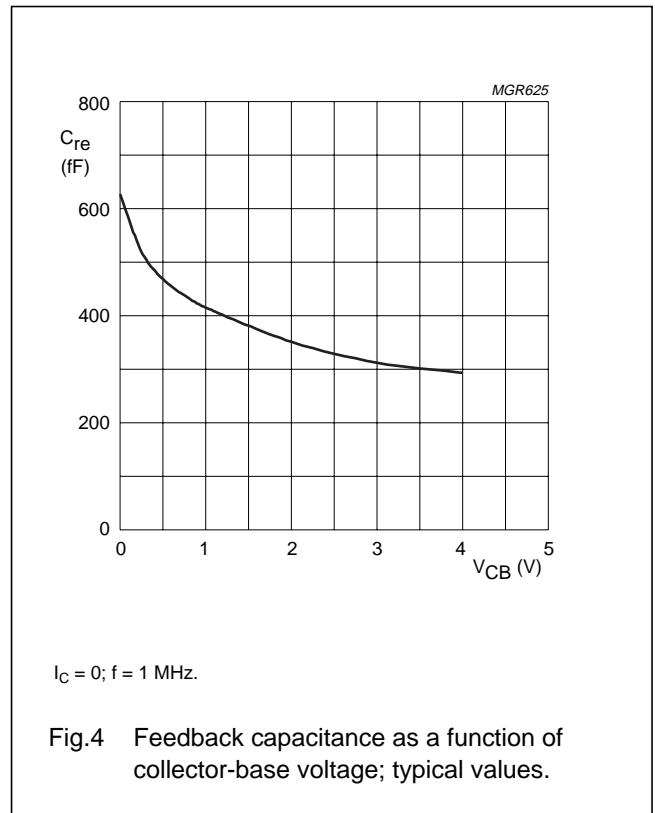
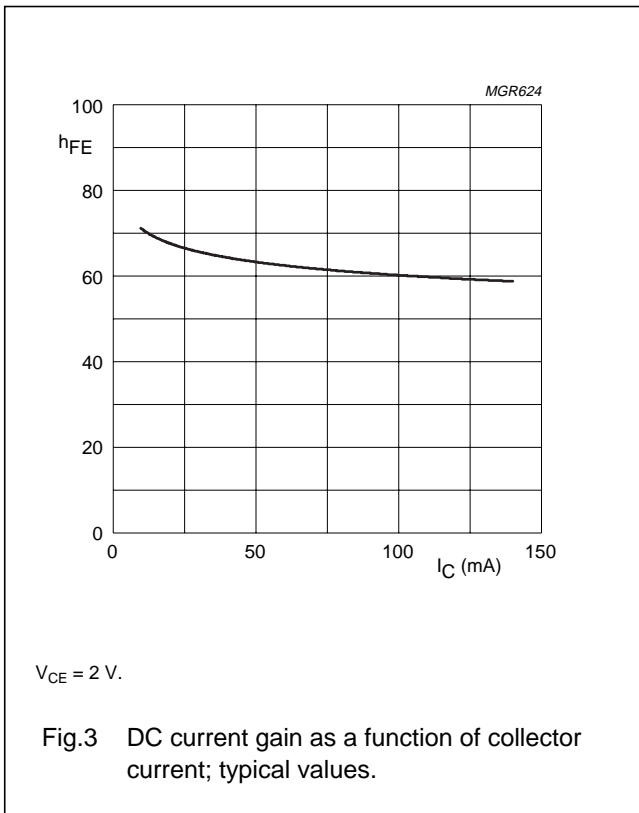
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 50\ \mu\text{A}; I_E = 0$	14.5	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 5\ \text{mA}; I_B = 0$	4.5	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 100\ \mu\text{A}; I_C = 0$	1	–	–	V
$I_{CBO}$	collector-base leakage current	$V_{CE} = 5\ \text{V}; V_{BE} = 0$	–	–	70	nA
$h_{FE}$	DC current gain	$I_C = 80\ \text{mA}; V_{CE} = 2\ \text{V}$ ; see Fig.3	40	60	100	
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 2\ \text{V}; f = 1\ \text{MHz}$	–	1.4	–	pF
$C_e$	emitter capacitance	$I_C = i_c = 0; V_{EB} = 0.5\ \text{V}; f = 1\ \text{MHz}$	–	2.2	–	pF
$C_{re}$	feedback capacitance	$I_C = 0; V_{CB} = 2\ \text{V}; f = 1\ \text{MHz}$ ; see Fig.4	–	340	–	fF
$f_T$	transition frequency	$I_C = 80\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; see Fig.5	–	21	–	GHz
$G_{max}$	maximum power gain; note 1	$I_C = 80\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; see Figs 7 and 8	–	16	–	dB
$ S_{21} ^2$	insertion power gain	$I_C = 80\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; see Fig.8	–	12	–	dB
F	noise figure	$I_C = 8\ \text{mA}; V_{CE} = 2\ \text{V}; f = 900\ \text{MHz}$ ; $\Gamma_S = \Gamma_{opt}$ ; see Fig.13	–	1.2	–	dB
		$I_C = 8\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz}$ ; $\Gamma_S = \Gamma_{opt}$ ; see Fig.13	–	1.8	–	dB
$P_{L1}$	output power at 1 dB gain compression	Class-AB; $\delta < 1 : 2$ ; $t_p = 5\ \text{ms}$ ; $V_{CE} = 3.6\ \text{V}; I_{CQ} = 1\ \text{mA}; f = 2\ \text{GHz}$	–	20	–	dBm
ITO	third order intercept point	$I_C = 80\ \text{mA}; V_{CE} = 2\ \text{V}; f = 2\ \text{GHz}$ ; $Z_S = Z_{S\ opt}; Z_L = Z_{L\ opt}$ ; note 2	–	28	–	dBm

## Notes

- $G_{max}$  is the maximum power gain, if  $K > 1$ . If  $K < 1$  then  $G_{max} = \text{MSG}$ ; see Figs 6, 7 and 8.
- $Z_S$  is optimized for noise;  $Z_L$  is optimized for gain.

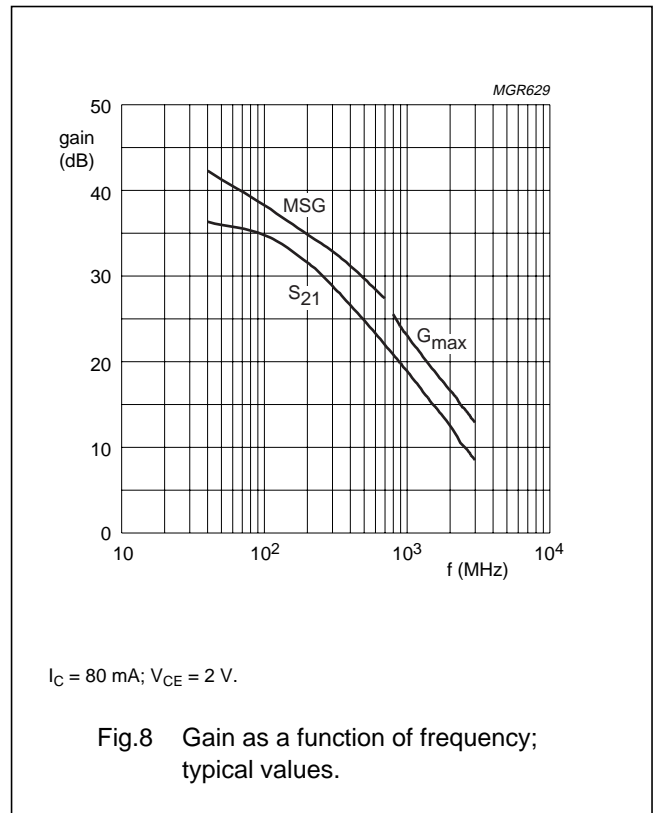
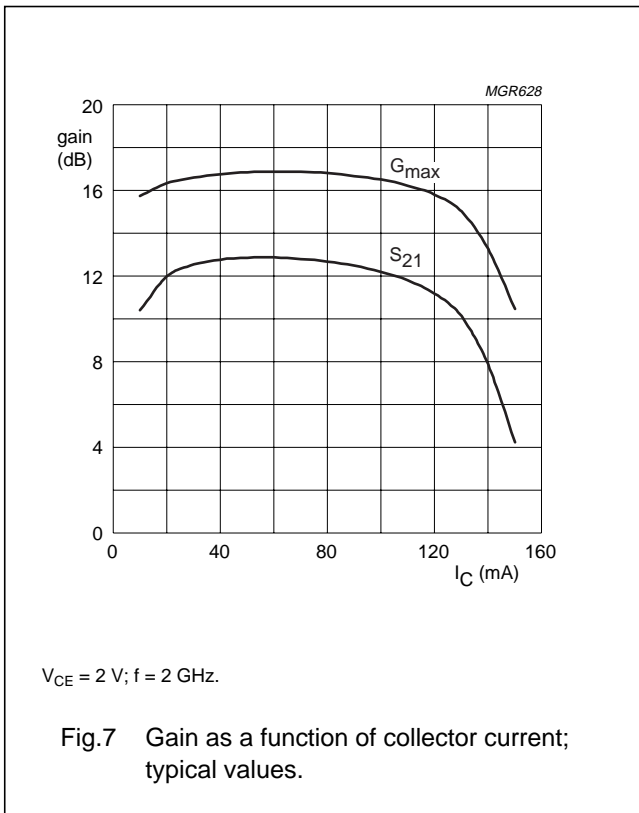
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BFG480W



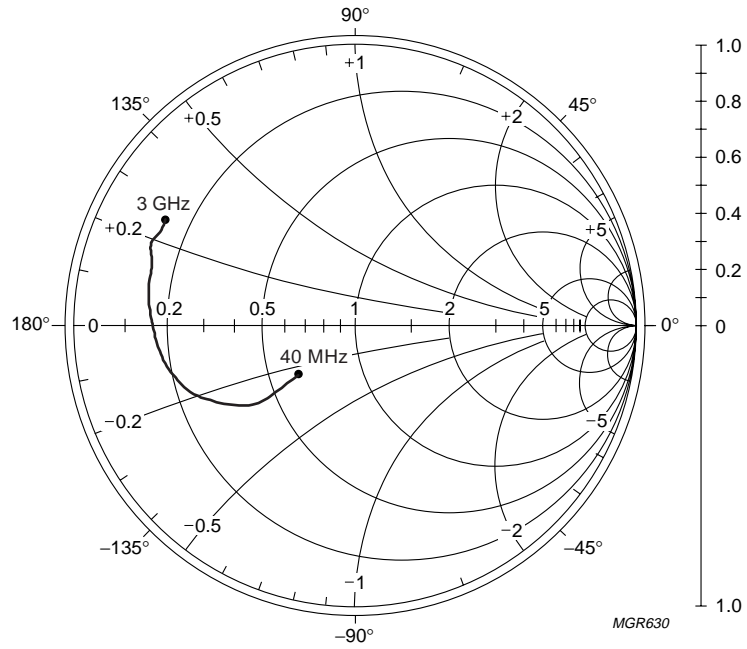
NPN wideband transistor

BFG480W



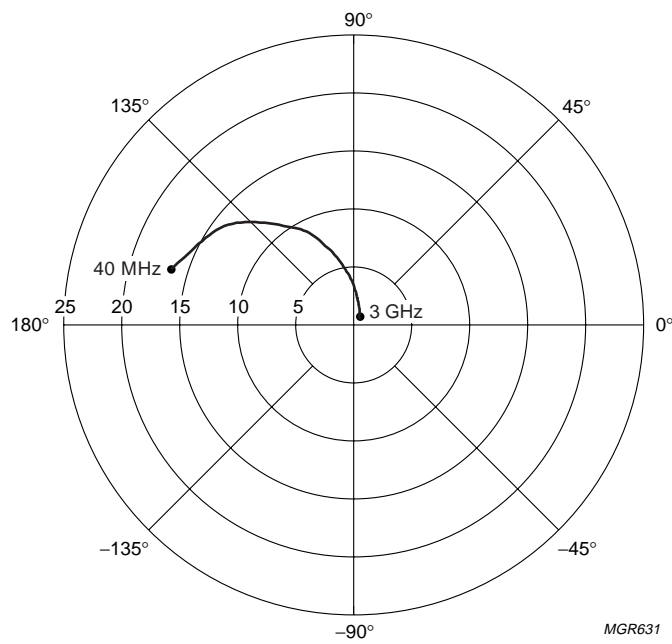
NPN wideband transistor

BFG480W



$I_C = 80 \text{ mA}; V_{CE} = 2 \text{ V}; Z_0 = 50 \Omega.$

Fig.9 Common emitter input reflection coefficient ( $S_{11}$ ); typical values.

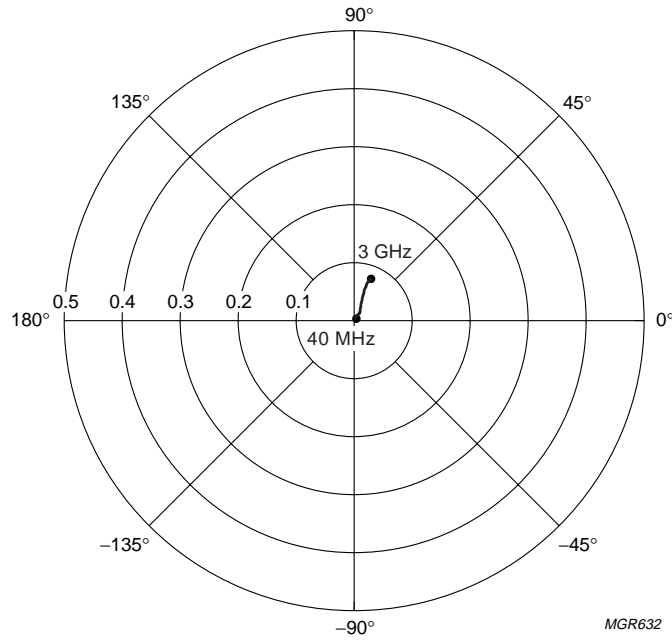


$I_C = 80 \text{ mA}; V_{CE} = 2 \text{ V}.$

Fig.10 Common emitter forward transmission coefficient ( $S_{21}$ ); typical values.

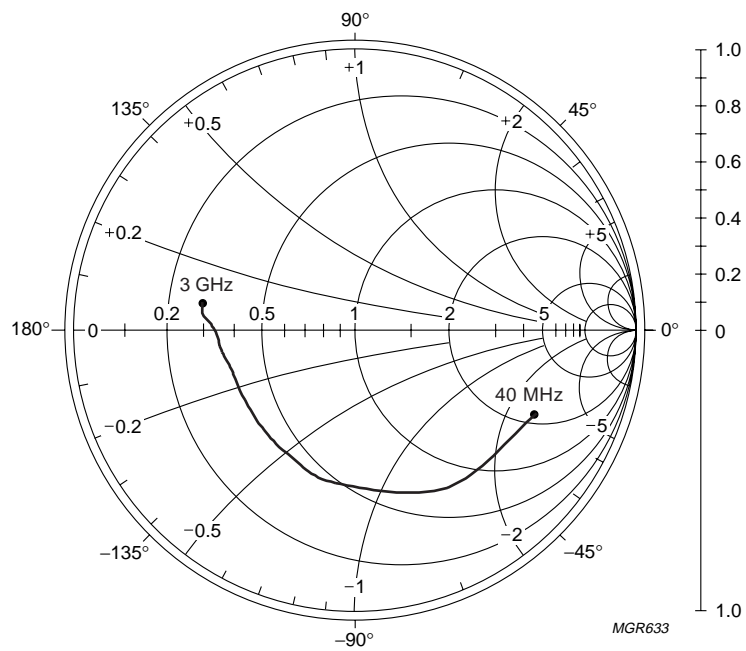
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$I_C = 80 \text{ mA}; V_{CE} = 2 \text{ V}.$

Fig.11 Common emitter reverse transmission coefficient ( $S_{12}$ ); typical values.



$I_C = 80 \text{ mA}; V_{CE} = 2 \text{ V}; Z_0 = 50 \Omega.$

Fig.12 Common emitter output reflection coefficient ( $S_{22}$ ); typical values.



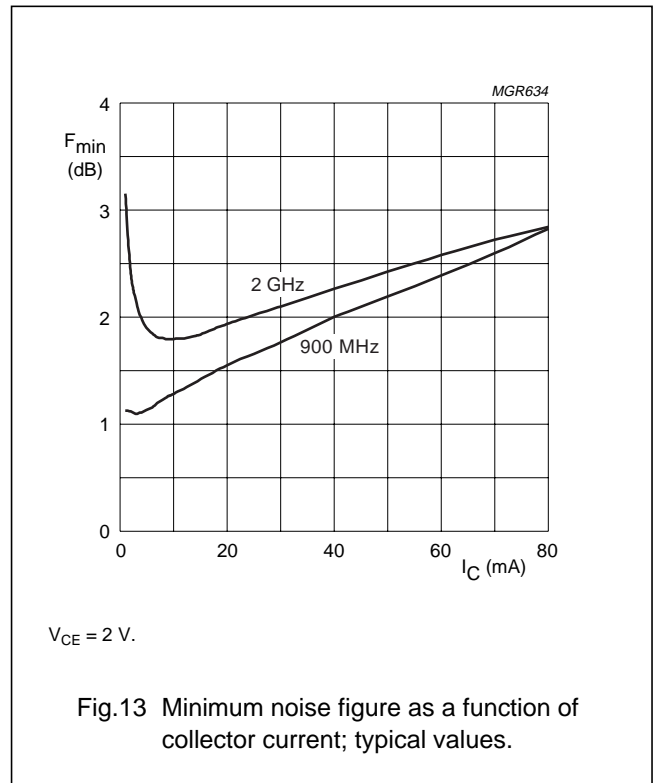
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BFG480W

Noise data

$V_{CE} = 2\text{ V}$ ; typical values.

f (MHz)	I <sub>C</sub> (mA)	F <sub>min</sub> (dB)	Γ <sub>mag</sub>	Γ <sub>angle</sub>	r <sub>n</sub> (Ω)
900	2	1.1	0.41	96.1	0.21
	4	1.1	0.31	106.6	0.14
	6	1.2	0.27	118.4	0.12
	8	1.2	0.26	131.7	0.10
	10	1.3	0.28	143.2	0.10
	20	1.6	0.39	166.2	0.07
	40	2.0	0.49	176.0	0.07
	60	2.3	0.57	179.5	0.07
2000	80	2.9	0.45	177.3	0.18
	2	2.4	0.57	171.9	0.09
	4	2.0	0.49	178.9	0.08
	6	1.8	0.46	-175.7	0.09
	8	1.8	0.44	-171.7	0.09
	10	1.8	0.43	-168.4	0.09
	12	1.8	0.44	-165.3	0.10
	14	1.8	0.44	-163.7	0.10
	20	1.9	0.46	-158.3	0.11
	40	2.3	0.52	-150.2	0.14
	60	2.6	0.56	-147.7	0.18
	80	2.8	0.60	-146.1	0.22



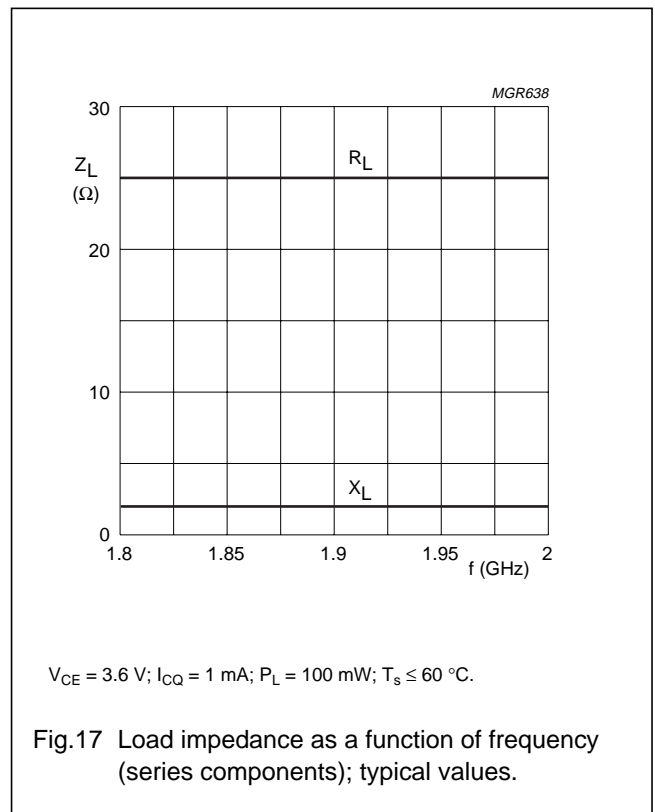
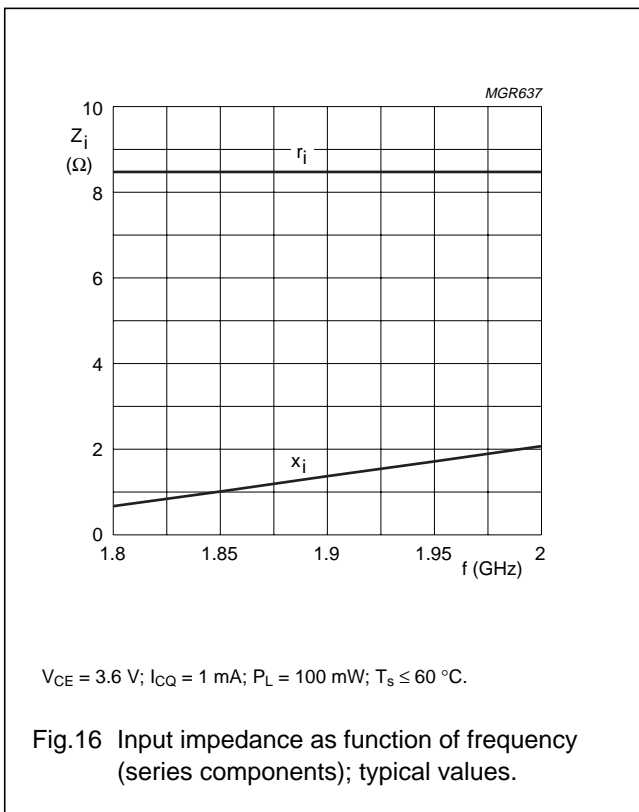
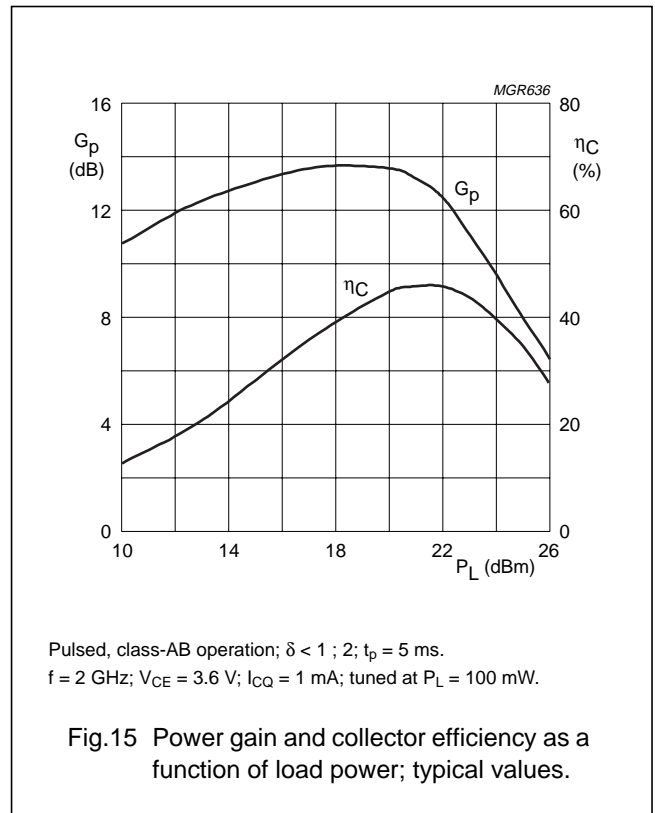
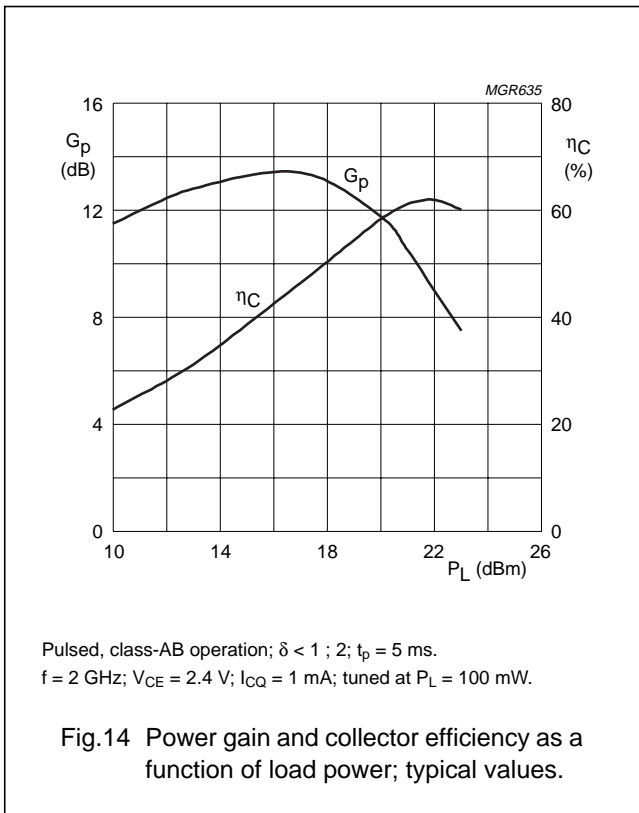
APPLICATION INFORMATION

RF performance at  $T_s \leq 60\text{ °C}$  in a common emitter test circuit (see Figs 18 and 19).

MODE OF OPERATION	f (GHz)	V <sub>CE</sub> (V)	I <sub>CQ</sub> (mA)	P <sub>L</sub> (mW)	G <sub>p</sub> (dB)	η <sub>c</sub> (%)
Pulsed; class-AB; δ < 1 : 2; t <sub>p</sub> = 5 ms	2	3.6	1	100	typ. 13.5	typ. 45

NPN wideband transistor

BFG480W



NPN wideband transistor

BFG480W

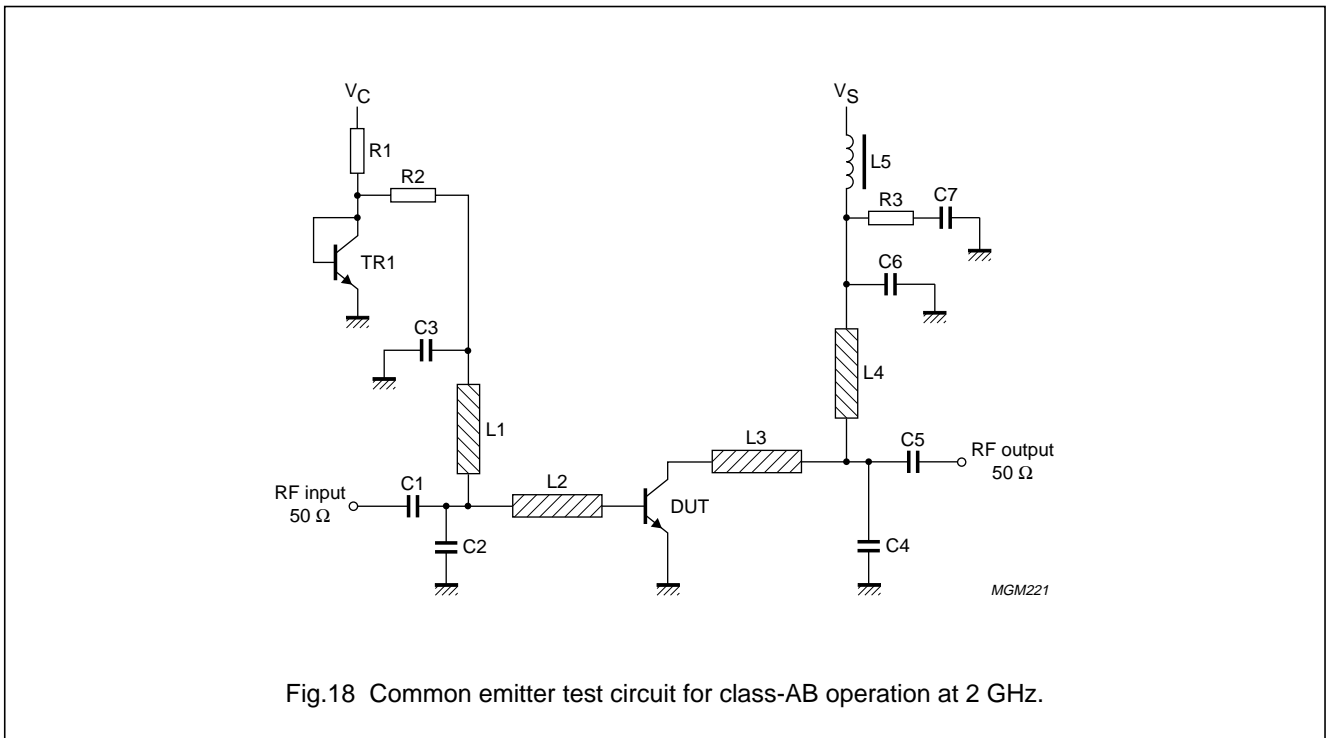


Fig.18 Common emitter test circuit for class-AB operation at 2 GHz.

List of components used in test circuit (see Figs 18 and 19)

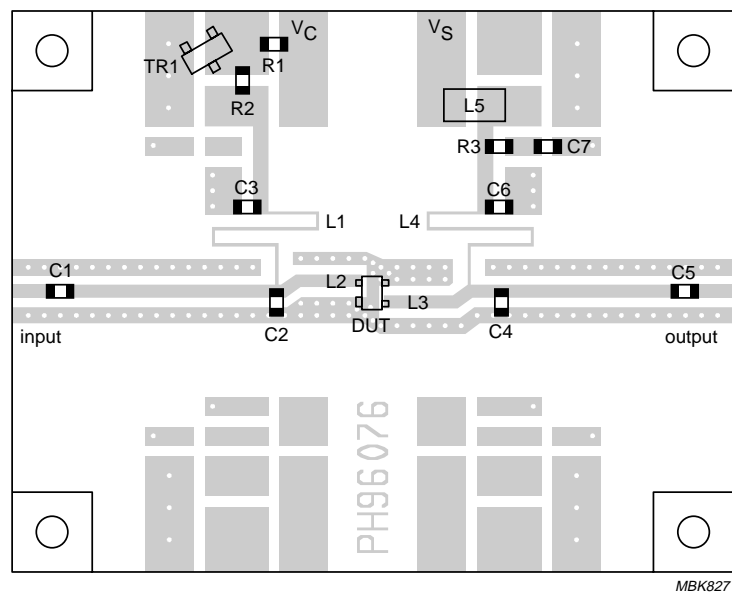
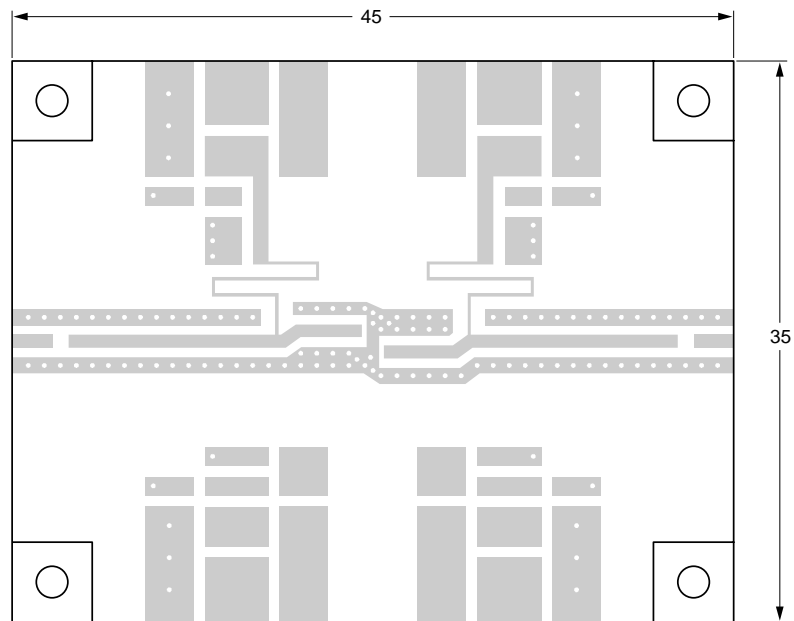
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C5	multilayer ceramic chip capacitor; note 1	24 pF		
C2, C4	multilayer ceramic chip capacitor; note 1	2 pF		
C3, C6	multilayer ceramic chip capacitor, note 1	15 pF		
C7	multilayer ceramic chip capacitor; note 1	1 nF		
L1, L4	stripline; note 2	100 Ω	18 x 0.2 mm	
L2	stripline; note 2	50 Ω	5 x 0.8 mm	
L3	stripline; note 2	50 Ω	6 x 0.8 mm	
L5	Grade 4S2 Ferroxcube chip bead			4330 030 36300
R1	metal film resistor	220 Ω; 0.4 W		
R2, R3	metal film resistor	10 Ω; 0.4 W		
TR1	NPN transistor	BC817		9335 895 20215

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- The striplines are on a double copper-clad printed-circuit board with PTFE fibre-glass dielectric ( $\epsilon_r = 6.15$ ,  $\tan \delta = 0.0019$ ); thickness 0.64 mm, copper cladding = 35  $\mu\text{m}$ .

NPN wideband transistor

BFG480W



Dimensions in mm.

The components are situated on one side of the copper-clad PTFE fibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.19 Printed-circuit board and component layout for 2 GHz class-AB test circuit in Fig.18.

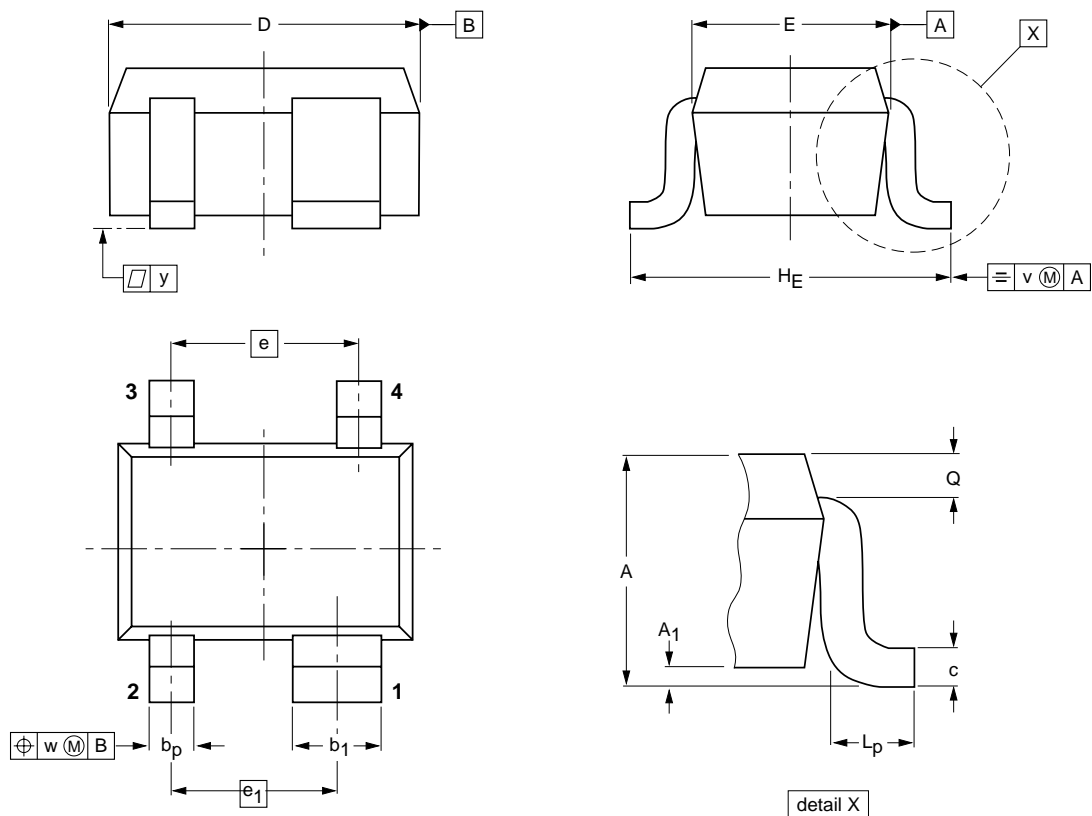
NPN wideband transistor

BFG480W

PACKAGE OUTLINE

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

## NPN wideband transistor

BFG480W

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**Indonesia:** PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

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**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

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**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

**Middle East:** see Italy

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**Pakistan:** see Singapore

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**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

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**Spain:** Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

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**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

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