



HIGH PERFORMANCE VRM USING L4990A,
FOR Pentium Pro® PROCESSOR

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SYSTEM DESCRIPTION

The actual generation of Pentium Pro® microprocessors, requires a power supply with a programmable output voltage that decreases with the increasing of the processor internal clock. At the same time higher output currents are required and superior load transient performance has to be supplied due to very high di/dt requests.

The VRM (Voltage Regulator Module) proposed (Fig 1) is a step down converter based on the L4990A, very fast current mode controller. A complete system solution is given and described. A connector with a standard VRM pinout is used, with 4 bit for Voltage Identify system, Power Good, Enable and constant limiting current functions are available. Output Over Voltage Protection is also available.

ELECTRICAL SPECIFICATION

Input Characteristics

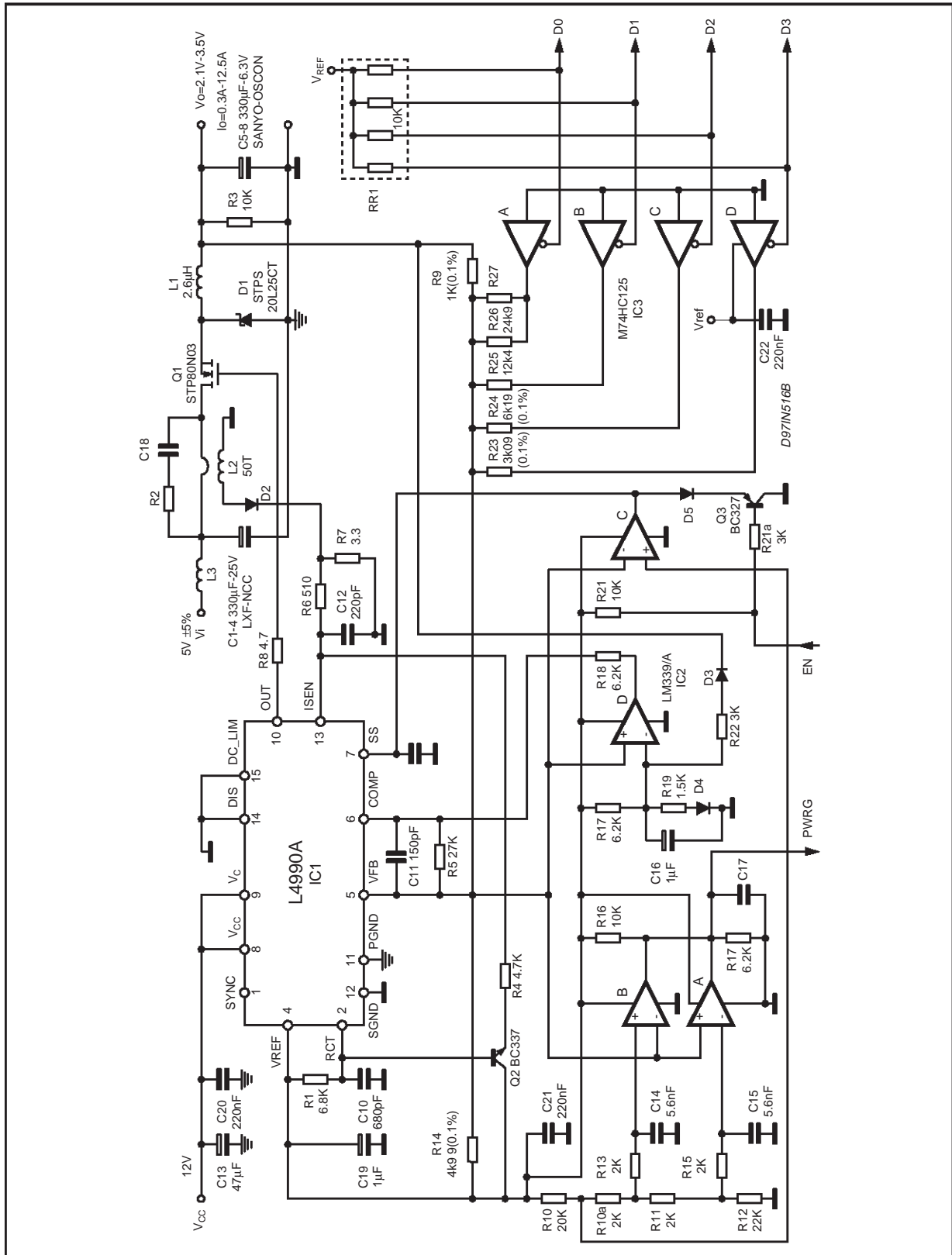
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_i	Input Voltage		4.75	5	5.25	V
di/dt	Slew Rate	Load Transient			0.04	A/ μ s
V_{bias}	Bias Voltage	$I_{12} = 45mA$	11.4	12	14	V

Output Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Output Voltage range	By 4 bits VID	2.1		3.5	V
V_{onm}	Nominal Output Voltage			2.9		V
I_o	Output Current		0.4		12.5	A
	Peak Current	Pulse by pulse mode	13			A
	Regulation	Including variation due to: - $I_o = \text{min-max}$ - V_o imital set point accuracy - Line regulation - Output ripple and noise - Load transient $dI_o/dt = 30A/\mu s$ - Temperature			± 5	%
η	Efficiency	$V_o = \text{min-max}; I_o = \text{min-max}$	70	85	93	%
	Output Over Voltage Protection	$V_o = \text{min-max}$		$1.18 \cdot V_o$		
	Foldback Current	Short circuit condition		12		A
fsw	Switching frequency			300		kHz

AN908 APPLICATION NOTE

Figure 1. Voltage Regulator Module.



Supply Voltages

The VRM is supplied by the 5V and the 12V standard outputs available from the conventional PC power supplies. The 12V is used here to supply the L4990A and the 5V power bus is used to supply the output power on the regulated DC output. An input inductor, L3, is necessary to limit the di/dt of the input current during load transients conditions.

This value must not exceed 0.1 A/us to prevent the intervention of protections on the main power supply.

Control Inputs

Enable: The module accept an open collector signal that disable the power supply in the low state. This function is realized by discharging the soft start capacitor.

This solution allows the module to restart with the soft start sequence.

Voltage Identification: The module is able to accept 4 open collectors input signals coming from the microprocessor.

Table 1 shows the VID0-3 code. The voltage identification is implemented with R23-26, R9 and R14 resistors, to allow to programm the converter output voltage at a value lower than the L4990A internal feedback reference, of 2.5V.

The four voltage identification bit are buffered with a 3-State buffer, 74HCT125.

Table 1.

VID3	VID2	VID1	VID0	Vo
1	1	1	1	no def
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

0 = Processor pin connected to ground
 1 = Processor pin Open

Output Control

Power Good Output: A PWRG signal is available. It's in the Low State when the programmed output voltage is inside the +/-10% of the nominal voltage, and in the High state outside the mentioned voltage range. This function is realized by using two comparators inside the quad LM339.

Internal Controls

Current limiting: The current limiting intervention is fixed at 13A to guarantee a good functionality at 12A continuous output current.

Behind 13A, the controller is going into pulse-by-pulse constant limiting current. A foldback type limiting current is also available.

In case a hiccup limiting current is accepted, the L4990A controller has this function on board.

Over Voltage Protection: a circuit is detecting an Overvoltage condition when output voltage is 18% above the nominal output voltage. In this case, the VRM is disabled.

Connector description

The connector is standard 40 pin, with a current capability of 3A/pin (type AMPMOD2 part number 532956-7 or equivalent) and the pinout is shown in Tab2.

Table 2. Connector pinout.

Pin #	ROW A	ROW B
1	Vin (5V)	Vin (5V)
2	Vin (5V)	Vin (5V)
3	Vin (5V)	Vin (5V)
4	Vin (12V)	Vin (12V)
5	Reserved	Reserved
6	Reserved	OUTEN
7	VID0	VID1
8	VID2	VID3
9	Reserved	PWRGD
10	Vo	GND
11	GND	Vo
12	Vo	GND
13	GND	Vo
14	Vo	GND
15	GND	Vo
16	Vo	GND
17	GND	Vo
18	Vo	GND
19	GND	Vo
20	Vo	GND

Figure 2. Efficiency vs. Output Current

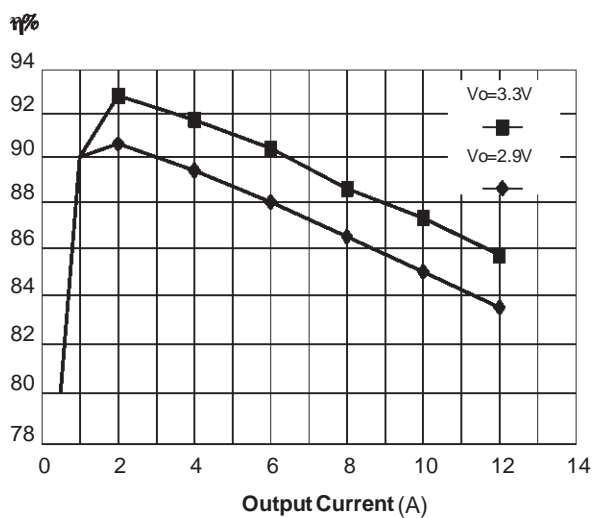


Figure 3. Input Current

CH1: I_{input} (5V) (1A/div)
 CH2: $V_o = 2.9V$ (50mV/div)
 Time: 10 μ s/div

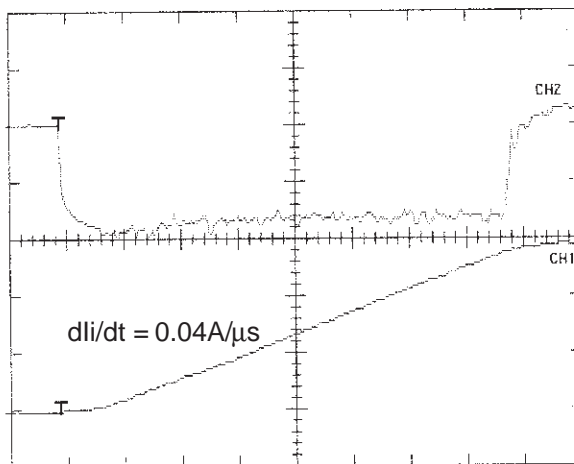


Figure 4. Load Transient

$I_o = 0.5A$ to 12A
 CH1: $V_o = 2.9V$ (50mV/div)
 CH2: I_o (5A/div)
 Time: 5 μ s/div

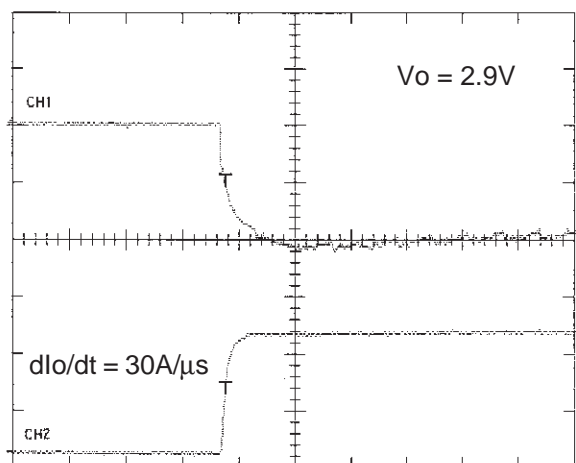
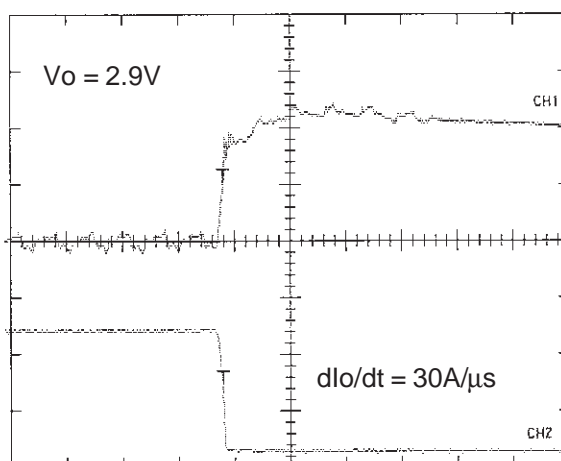


Figure 5. Load Transient

$I_o = 12A$ to 0.5A
 CH1: $V_o = 2.9V$ (50mV/div)
 CH2: I_o (5A/div)
 Time: 5 μ s/div



COMPONENT LIST

R1	6.8k	R19	3.6k	C16	1 μ F/50V
R2	1.8	R20	2.7k	C17	220nF
R3	10k	R21	10k	C18	1.2nF
R4	4.7	R21a	3k	C19	1 μ F/50V
R5	27k	R22	3k	C20-22	220nF
R6	510	R23	3.09k (0.1%)	Q1	STP80N03L-06
R7	3.3	R24	6.19k (0.1%)	Q2	BC337
R8	4.7	R25	12.4k	Q3	BC327
R9	1k	R26	24.9k	D1	STPS20L25CT
R10	20k	R27	xx	D2-5	1N4148
R10a	2k	RR1	10k (5+1)	IC1	L4990A
R11	2k	C1-4	470 μ F/25V HFQ Panasonic	IC2	LM339
R12	22k	C5-8	330 μ F/6.3V SANYO-Oscon	IC3	M74HC125
R13	2k	C9	33nF	L1	77120(6T) Magnetics
R14	4.99k (0.1%)	C10	680pF	L2	40705-TC(50T) Magnetics
R15	2k	C11	150pF	L3	T38-52(4T) Micrometals
R16	10k	C12	220pF		
R17	6.2k	C13	47 μ F/50V		
R18	6.2k	C14-15	5.6nF		

Figure 6. PCB Layout - Xerography (77.47 x 78.74mm)

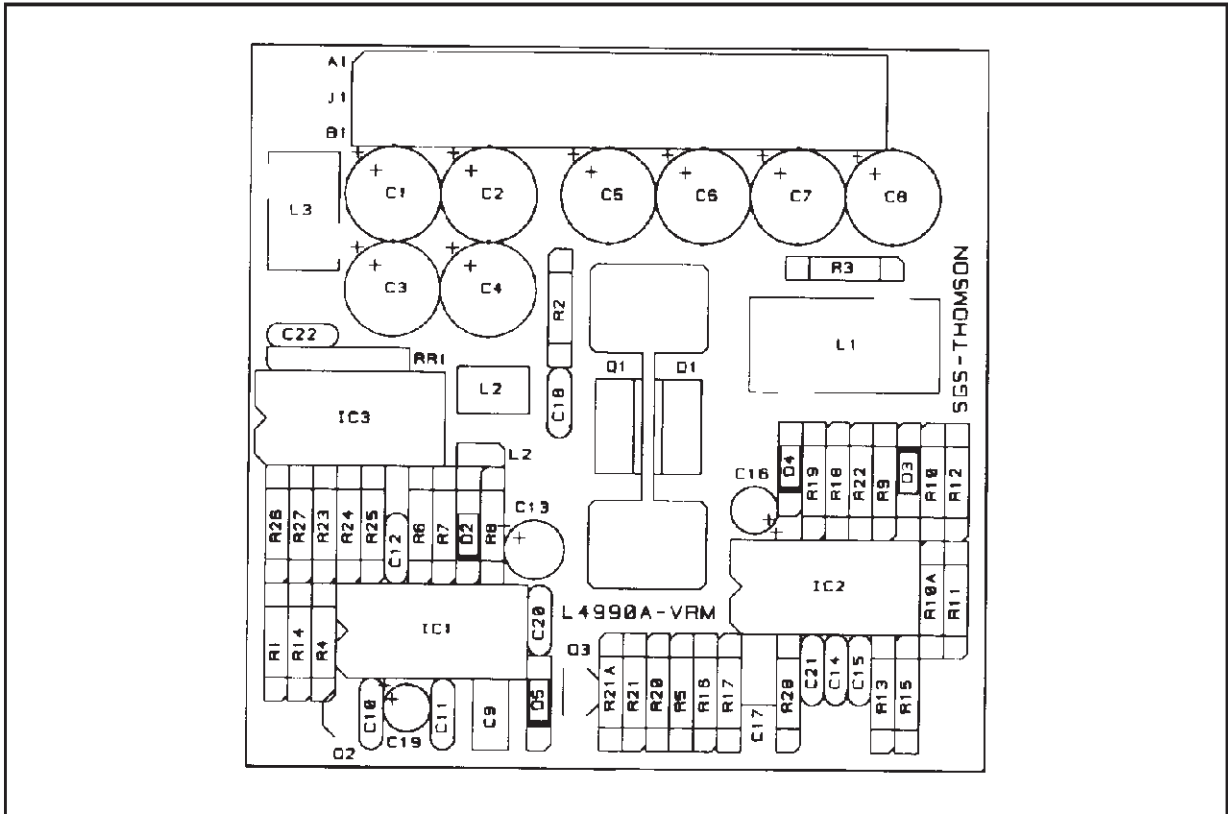


Figure 7. PCB Layout - Layer 1 (77.47 x 78.74mm)

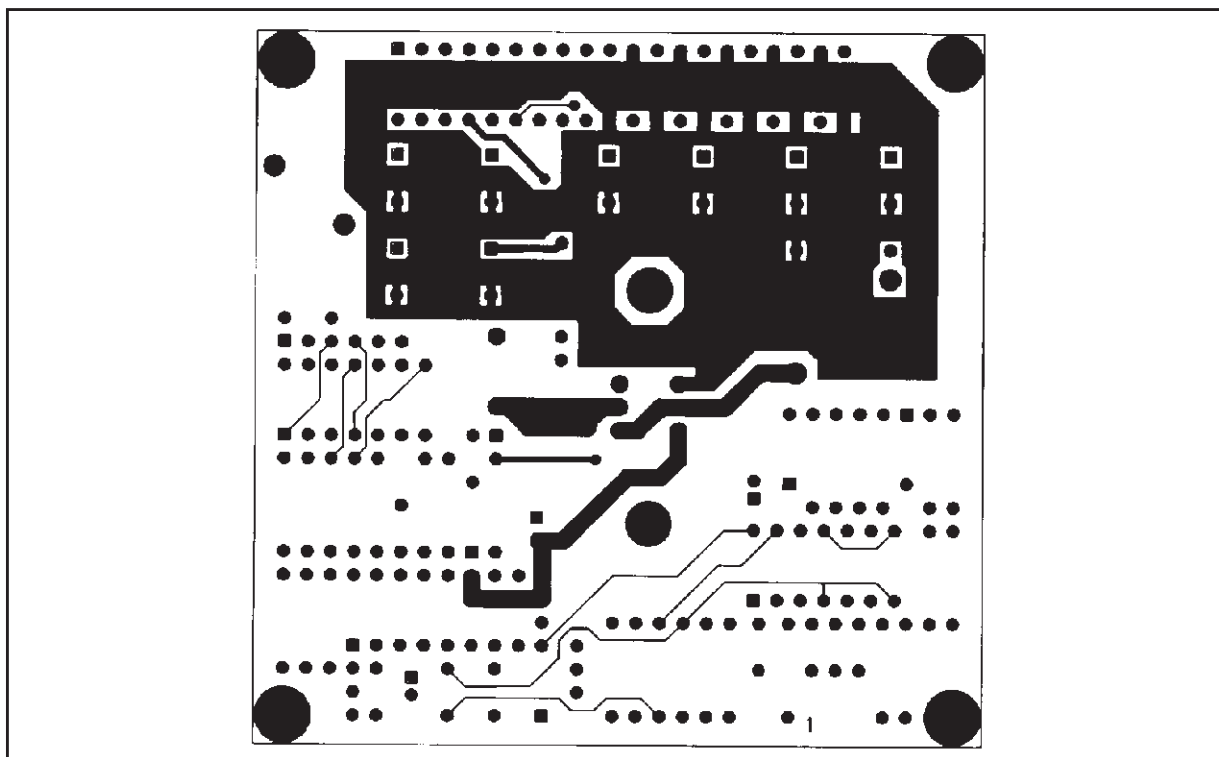


Figure 8. PCB Layout - Layer 2 (77.47 x 78.74mm)

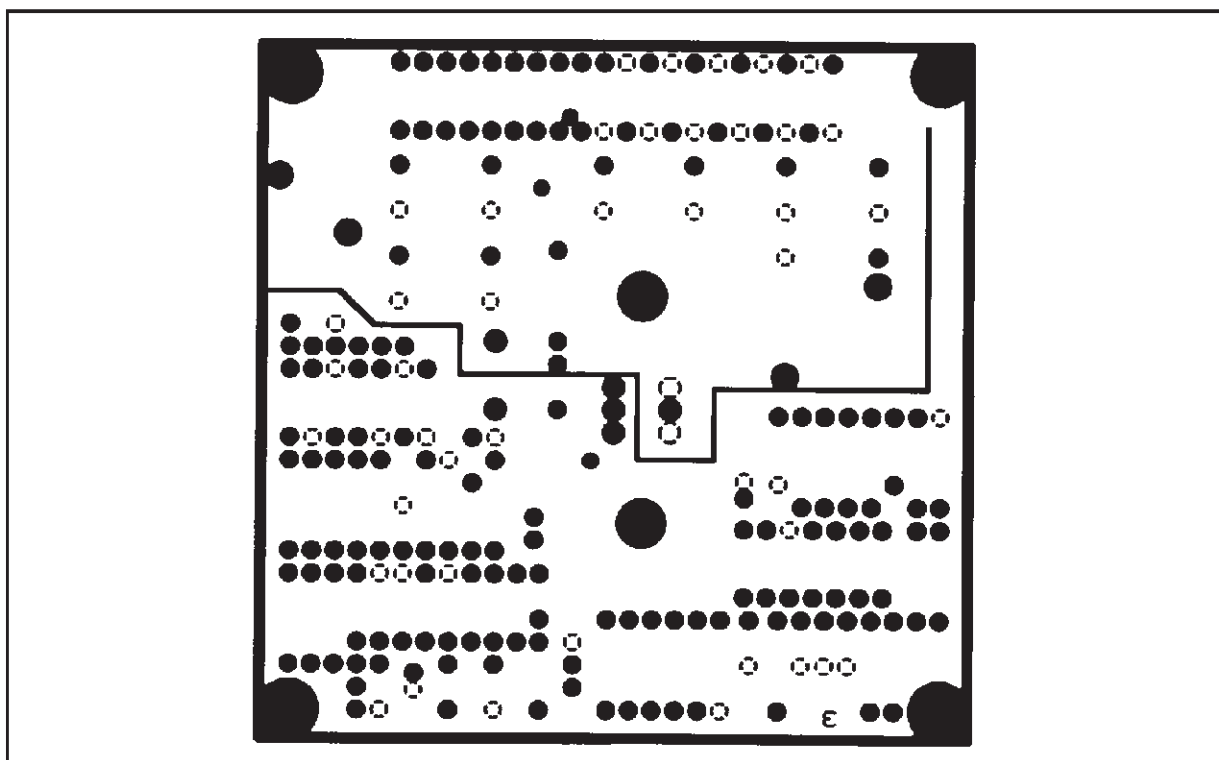


Figure 9. PCB Layout - Layer 3 (77.47 x 78.74mm)

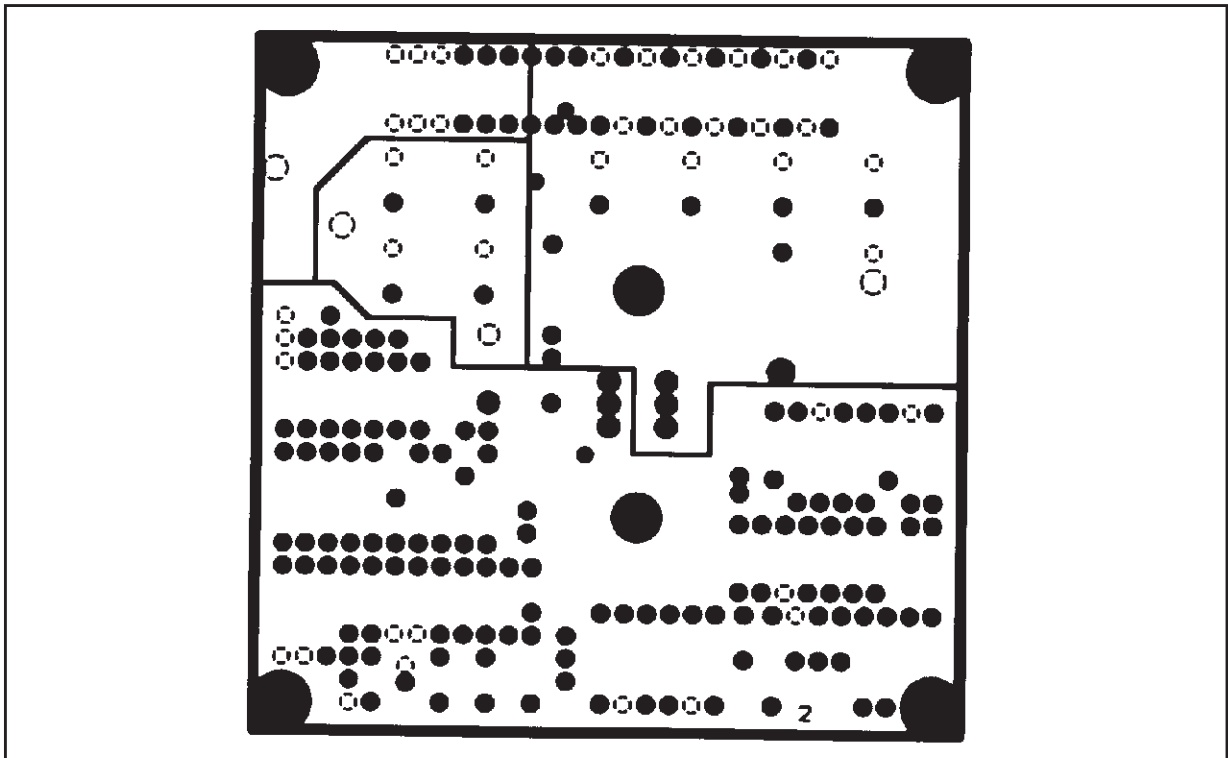
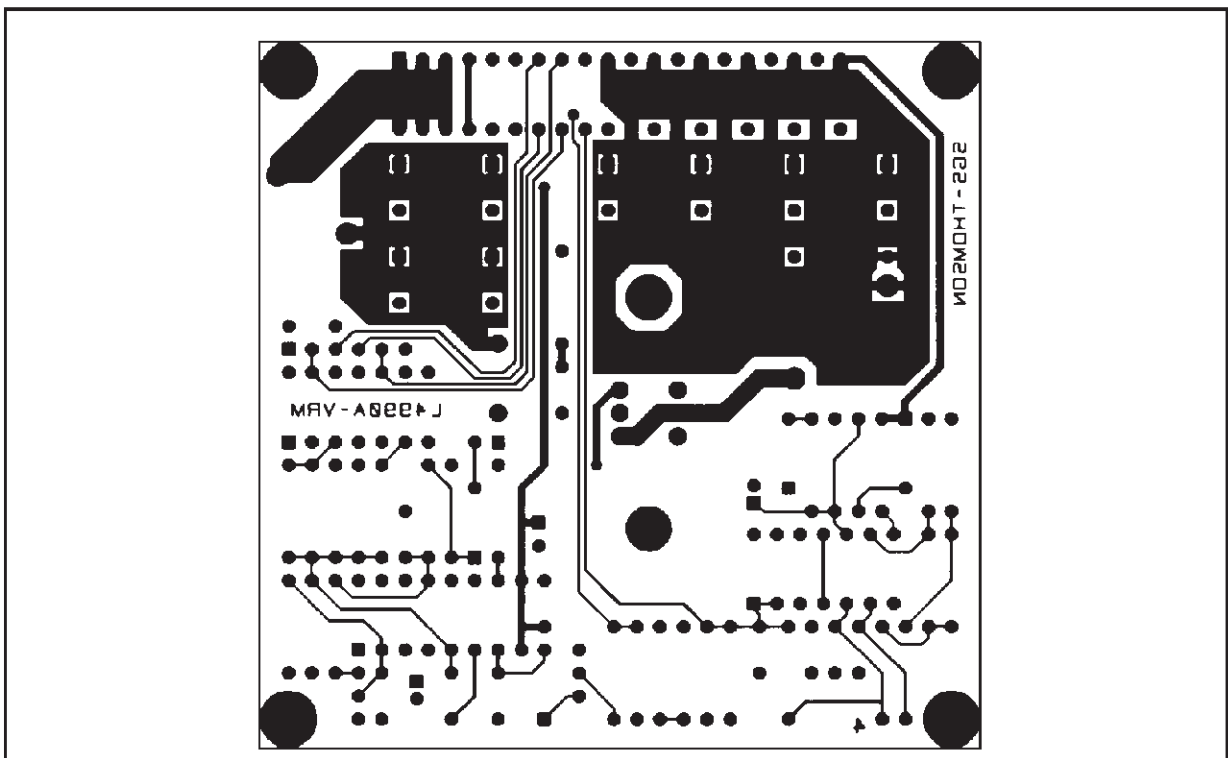


Figure 10. PCB Layout - Layer 4 (77.47 x 78.74mm)



APPLICATION IDEAS

Figure 11. Voltage Mode Regulator.

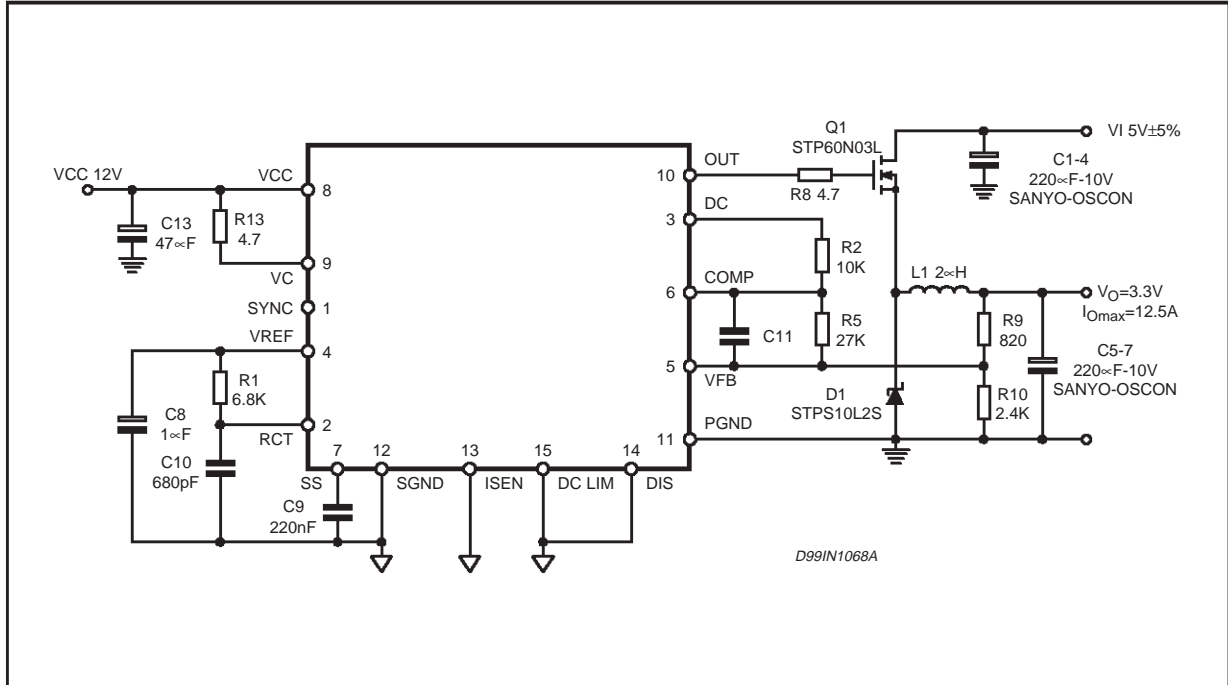
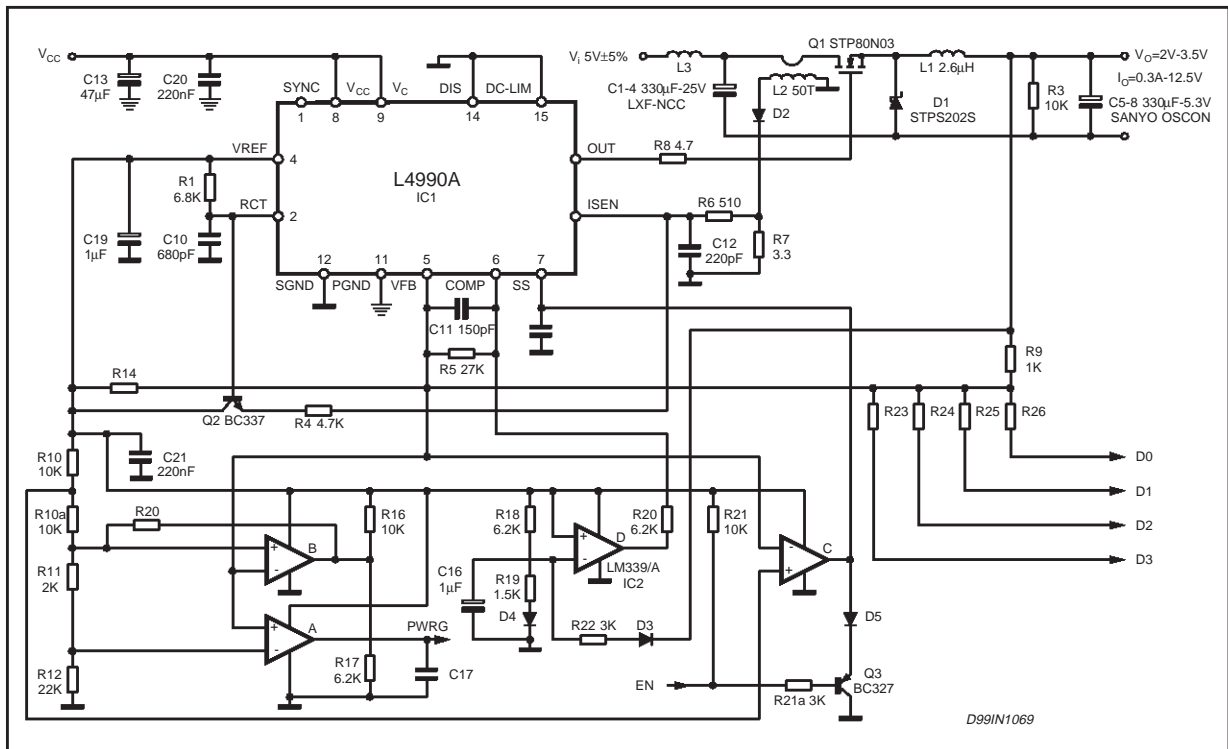


Figure 12. Simplified Schematic.



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