SGS-THOMSON MICROELECTRONICS

STHV102

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

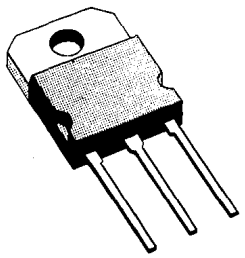
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STHV102	1000 V	3.5 Ω	4.2 A

- 1000 V - VERY HIGH VOLTAGE FOR SMPS
- EASY DRIVE - REDUCED COST AND SIZE
- ULTRA FAST SWITCHING
- HIGH RESOLUTION CTV DEFLECTION

INDUSTRIAL APPLICATIONS:

- SINGLE TRANSISTOR HIGH VOLTAGE SWITCH
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include single transistor forward and flyback converters and lamp ballast. They are also used in high voltage CTV EHT supplies, interfaces to thyristor and power transistors operating from 380V and 440V A.C. supplies and resonant converters operating up to 500kHz.



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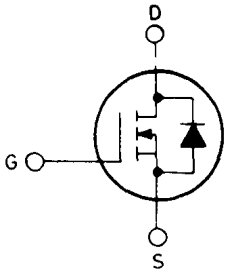
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	1000	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	4.2	A
I_D	Drain current (cont.) at $T_c=100°C$	2.6	A
I_{DM} (•)	Drain current (pulsed)	16	A
P_{tot}	Total dissipation at $T_c<25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

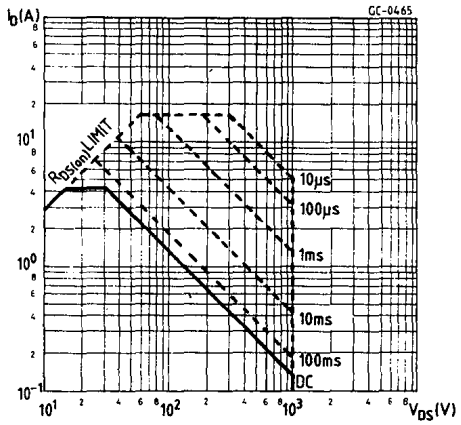
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	1000			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2 A			3.5	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		900 150 90	1200 250 110	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 400 V V_i = 10 V (see test circuit)	I_D = 2 A R_i = 50 Ω		40 100 300 100		ns ns ns ns
Q_g	Total gate Charge	V_{DD} = 500 V V_{GS} = 10 V	I_D = 6 A			70	nC

ELECTRICAL CHARACTERISTICS (Continued)

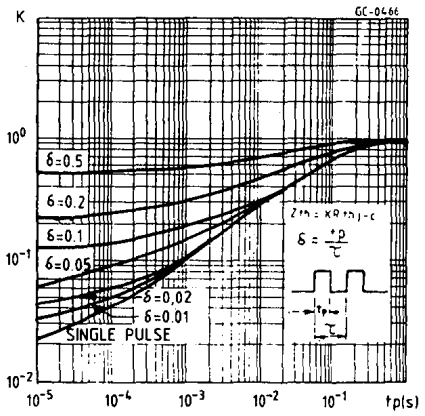
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				4.2 16	A A
V_{SD} Forward on voltage	I_{SD} = 4.2 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time Q_{rr} Reverse recovery charge	I_{SD} = 4.2 A V_{GS} = 0 di/dt = 100 A/μs		1000 15		ns μC

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

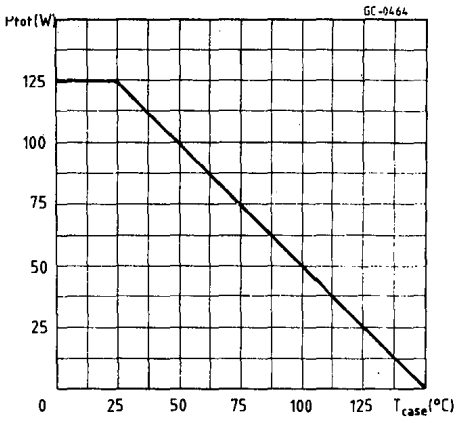
Safe operating areas



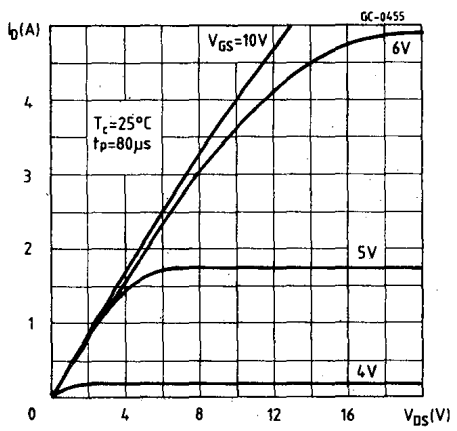
Thermal impedance



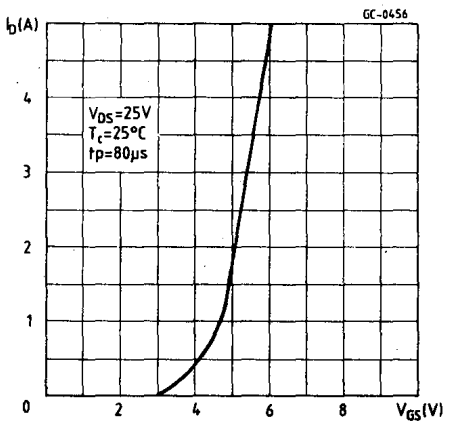
Derating curve



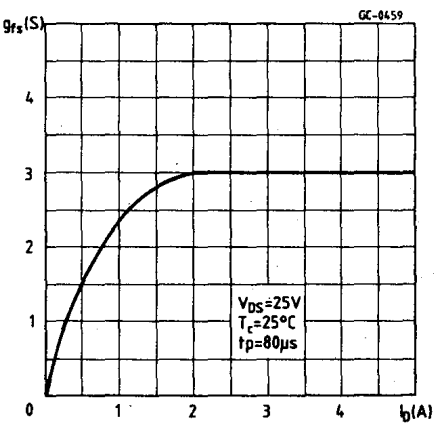
Output characteristics



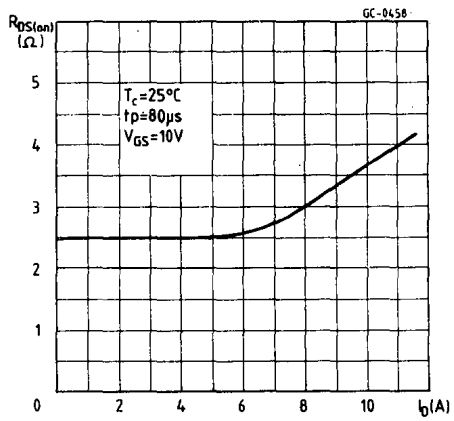
Transfer characteristic



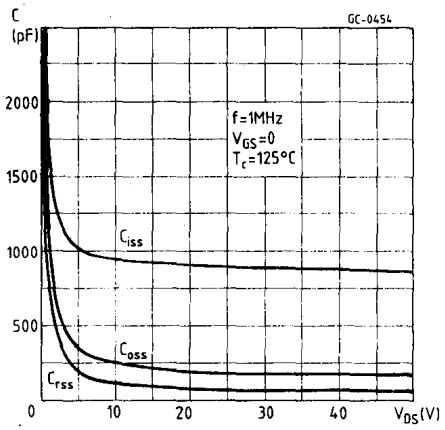
Transconductance



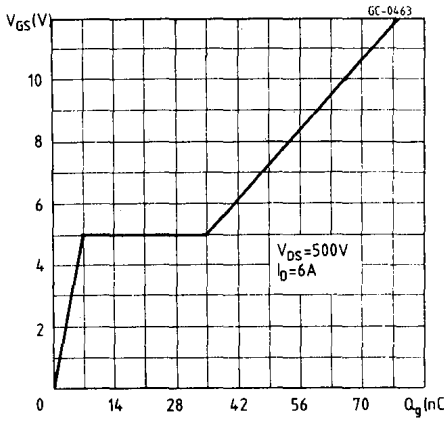
Static drain-source on resistance



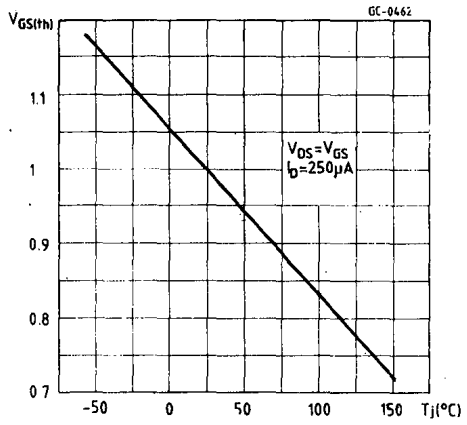
Capacitance variation



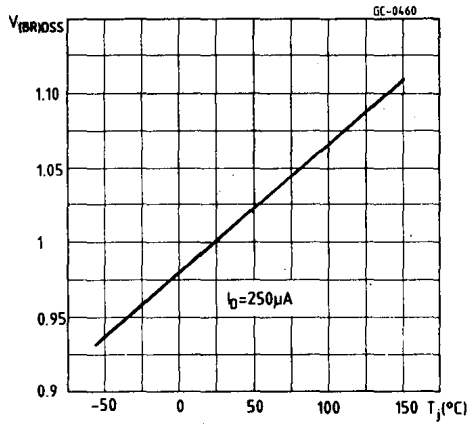
Gate charge vs gate-source voltage



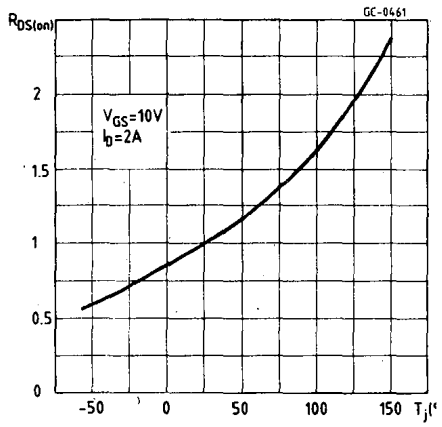
Normalized gate threshold voltage vs temperature



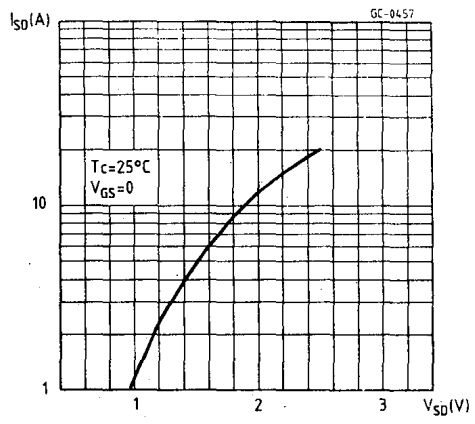
Normalized breakdown voltage vs temperature



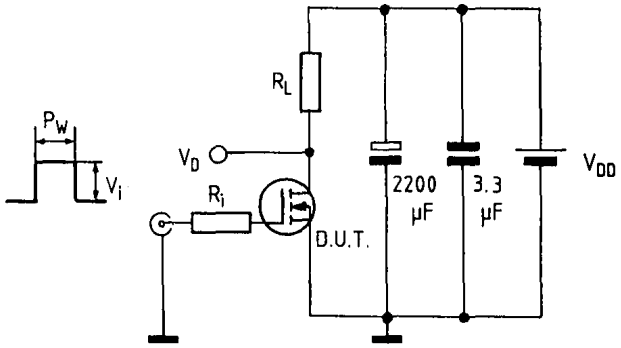
Normalized on resistance vs temperature



Static drain diode forward characteristic

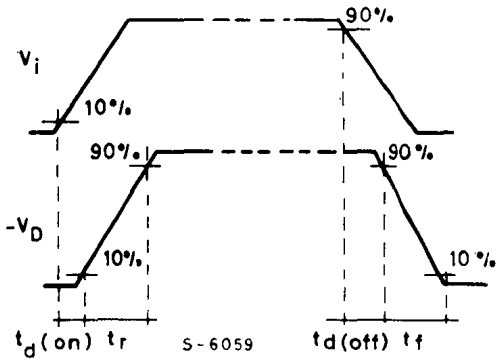


Switching times test circuit for resistive load

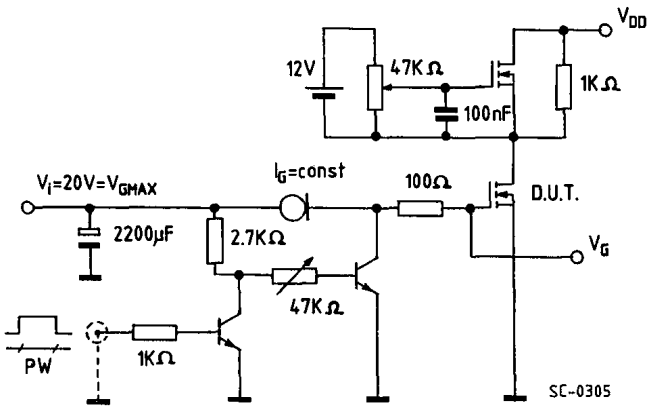


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit