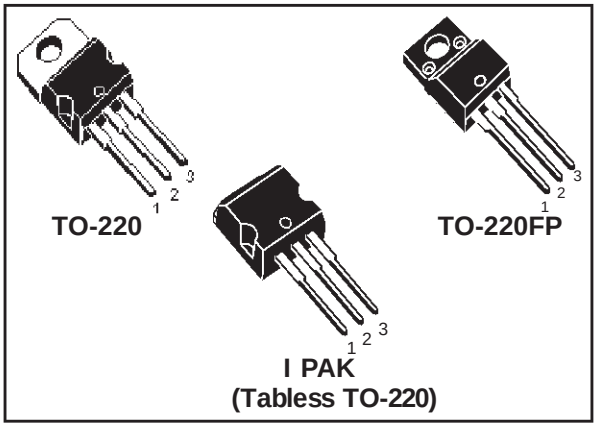
STP6NC90Z - STP6NC90ZFP
STB6NC90Z-1

N-CHANNEL 900V - 1.55Ω - 5.4A TO-220/TO-220FP/I PAK
Zener-Protected PowerMESH™ III MOSFET

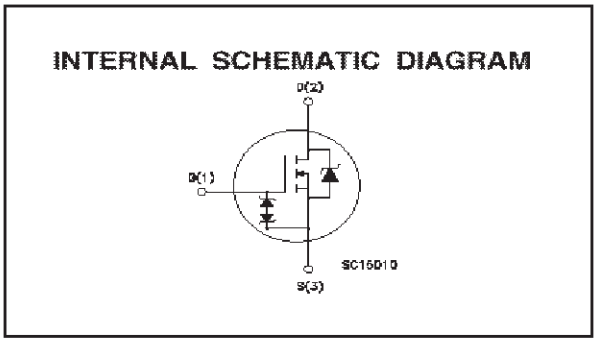
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP6NC90Z/FP	900V	< 1.9 Ω	5.4 A
STB6NC90Z-1	900V	< 1.9 Ω	5.4 A

- TYPICAL R_{DS}(on) = 1.55Ω
- EXTREMELY HIGH dv/dt AND CAPABILITY GATE TO - SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW GATE INPUT RESISTANCE
- GATE CHARGE MINIMIZED



DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.



APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)6NC90Z(-1)	STP6NC90ZFP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	900		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	900		V
V_{GS}	Gate- source Voltage	± 25		V
I_D	Drain Current (continuos) at T_C = 25°C	5.4	5.4(*)	A
I_D	Drain Current (continuos) at T_C = 100°C	4.9	4.9(*)	A
I_{DM} (1)	Drain Current (pulsed)	21	21	A
P_{TOT}	Total Dissipation at T_C = 25°C	135	40	W
	Derating Factor	1.08	0.32	W/°C
I_{GS}	Gate-source Current	±50		mA
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=15KΩ)	3		KV
dv/dt	Peak Diode Recovery voltage slope	3		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	--	2000	V
T_{stg}	Storage Temperature	–65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤5.4A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}

(2) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 / I PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.93	3.13	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.4	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	356	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	900			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 1 mA, V_{GS} = 0		1		V/°C
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 3 A		1.55	1.9	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 3A		5.7		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2290		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			15		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 450 V, I_D = 3 A		24		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		8		ns
Q_g	Total Gate Charge	V_{DD} = 720V, I_D = 6A,		42	58.8	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V		13		nC
Q_{gd}	Gate-Drain Charge			15		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 720V, I_D = 6 A,		10		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		11		ns
t_c	Cross-over Time			14		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				5.4	A
I_{SDM} (2)	Source-drain Current (pulsed)				21.6	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 6 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 6 A, di/dt = 100A/µs,		680		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 40 V, T_j = 150°C (see test circuit, Figure 5)		7.14		µC
I_{RRM}	Reverse Recovery Current			21		A

GATE-SOURCE ZENER DIODE

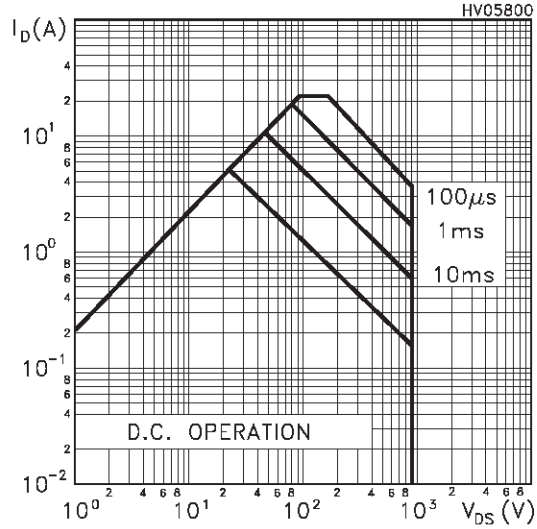
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	25			V
αT	Voltage Thermal Coefficient	T=25°C Note(3)		1.3		10^{-4}/°C
Rz	Dynamic Resistance	I_D = 50 mA, V_{GS} = 0		90		Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $\Delta V_{BV} = \alpha T\ (25°\text{-}T)\ BV_{GSO}(25°)$

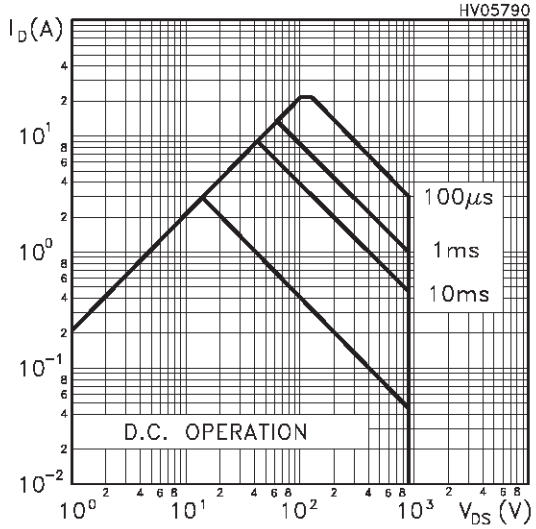
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to souce. In this respect the 25V Zener voltage is appropiate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

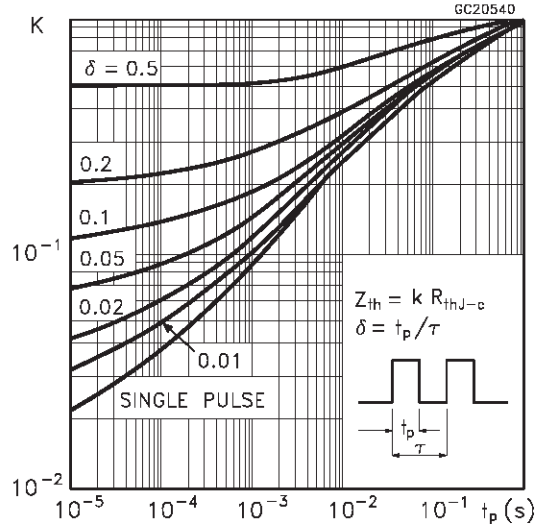
Safe Operating Area For TO-220 / I PAK



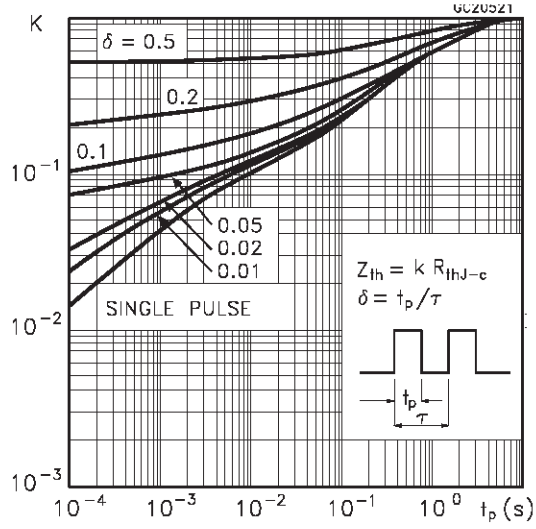
Safe Operating Area For TO-220FP



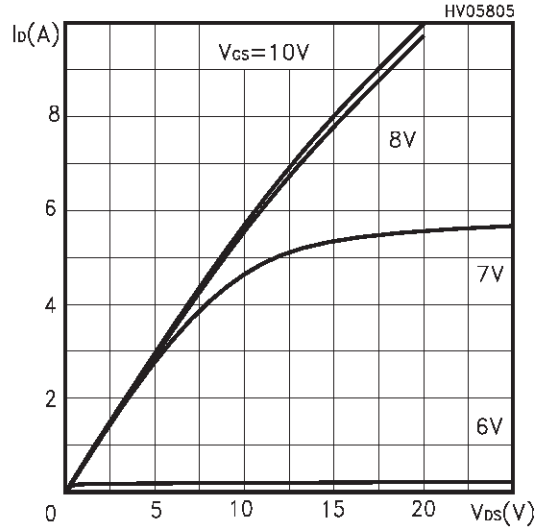
Thermal Impedance For TO-220 / I PAK



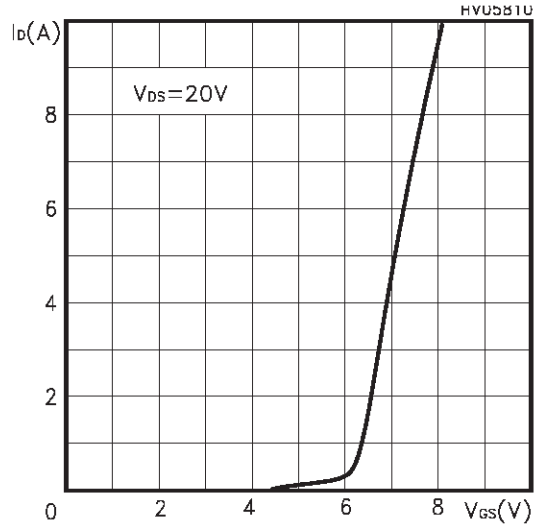
Thermal Impedance For TO-220FP



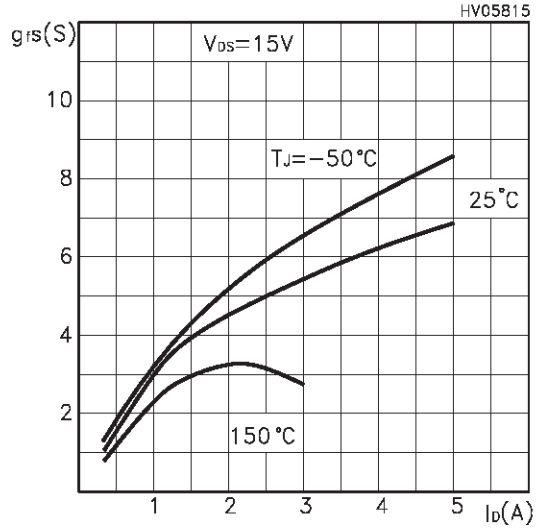
Output Characteristics



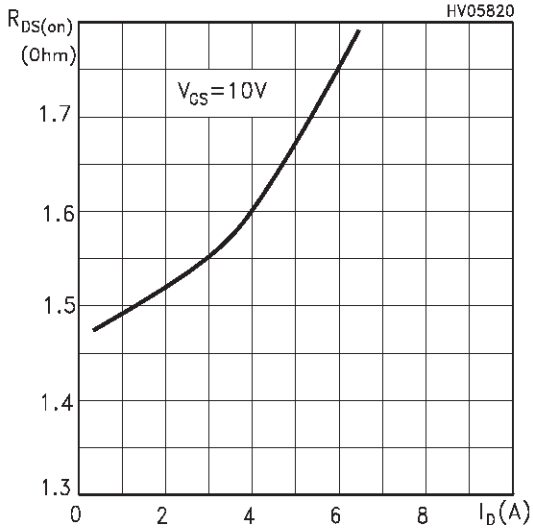
Transfer Characteristics



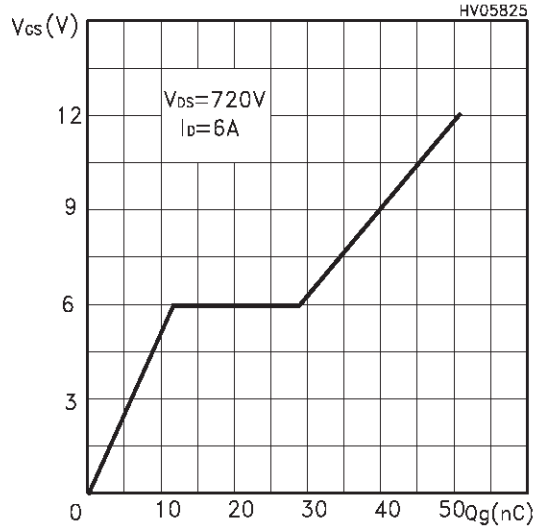
Transconductance



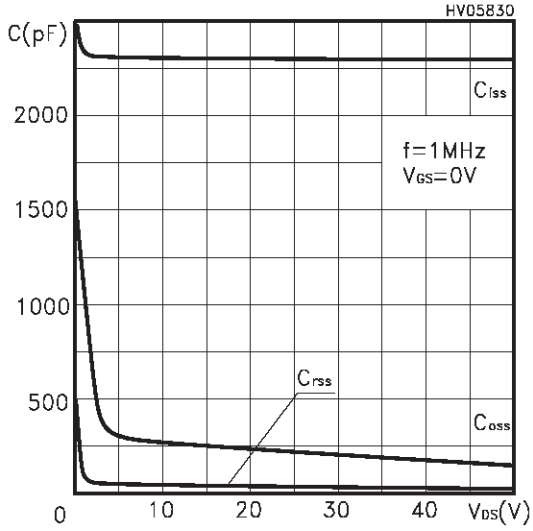
Static Drain-source On Resistance



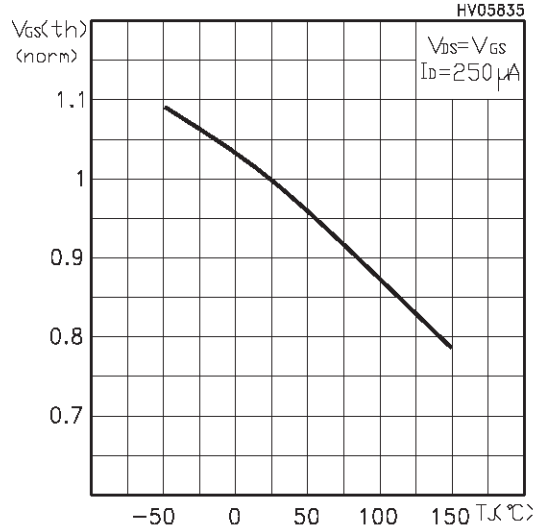
Gate Charge vs Gate-source Voltage



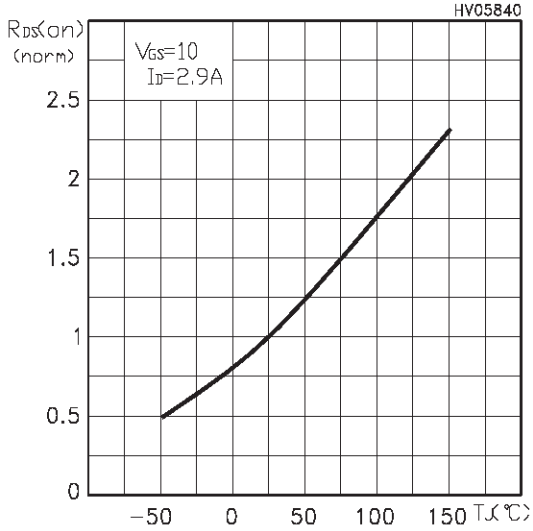
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

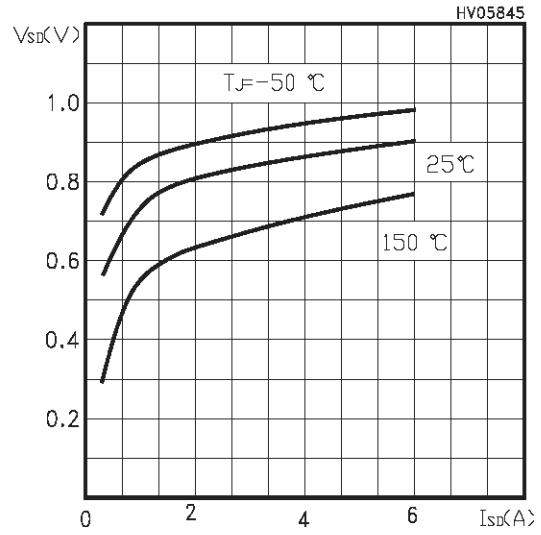


Fig. 1: Unclamped Inductive Load Test Circuit

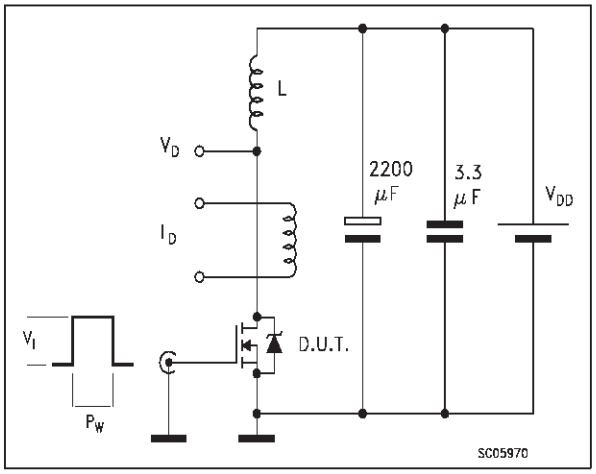


Fig. 2: Unclamped Inductive Waveform

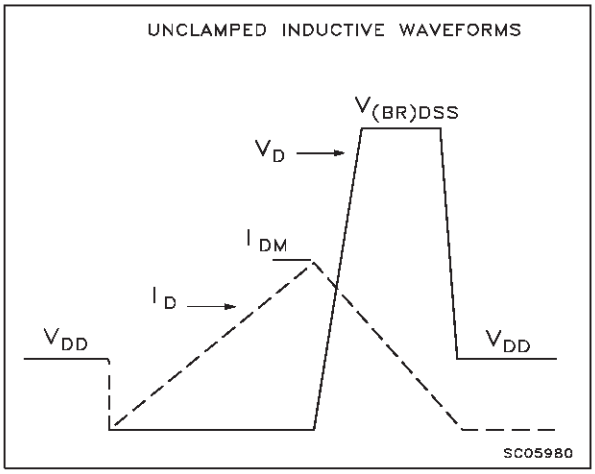


Fig. 3: Switching Times Test Circuits For Resistive Load

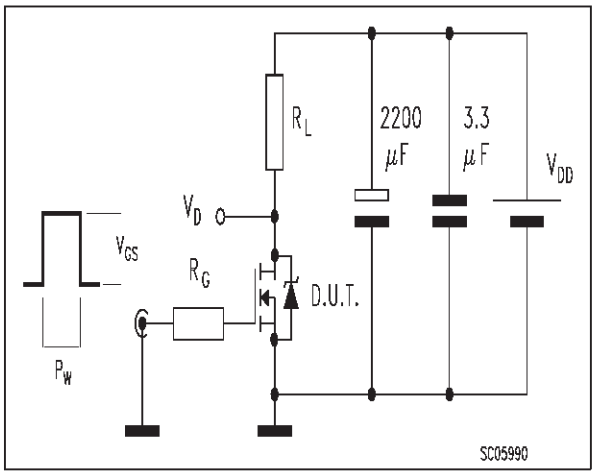


Fig. 4: Gate Charge test Circuit

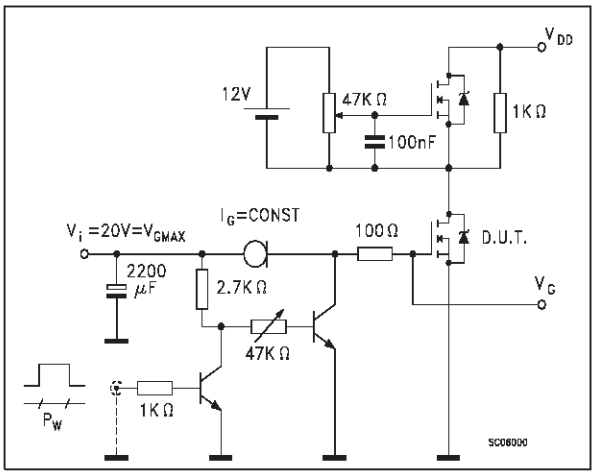
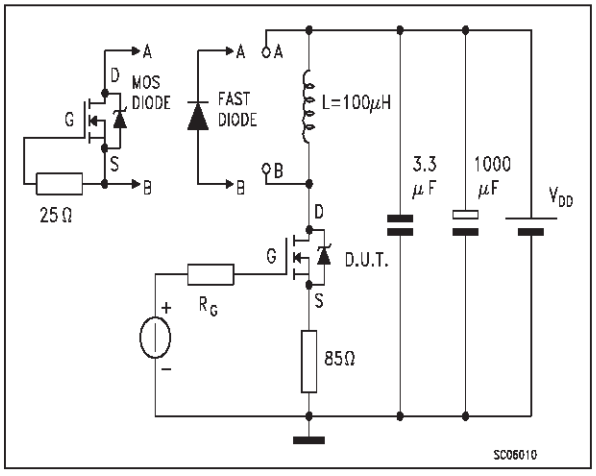


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151