



Dual P-Channel 30-V (D-S) MOSFET

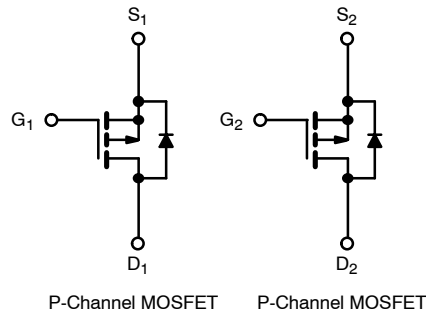
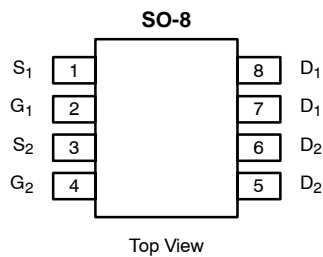
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.032 @ $V_{GS} = -10$ V	-6.3
	0.045 @ $V_{GS} = -4.5$ V	-5.3

FEATURES

- TrenchFET® Power MOSFET



Pb-free
Available



Ordering Information: Si4925DY
Si4925DY-T1 (with Tape and Reel)
Si4925DY—E3 (Lead (Pb)-Free)
Si4925DY-T1—E3 (Lead (Pb)-Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-6.3	-4.7	A
		$T_A = 70^\circ\text{C}$	-5.0	-3.7	
Pulsed Drain Current	I_{DM}	-40			
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	-0.9		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2	1.1	W
		$T_A = 70^\circ\text{C}$	1.3	0.70	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typ	Max	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	45	62.5	$^\circ\text{C/W}$
		Steady-State	85	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	28	35		

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

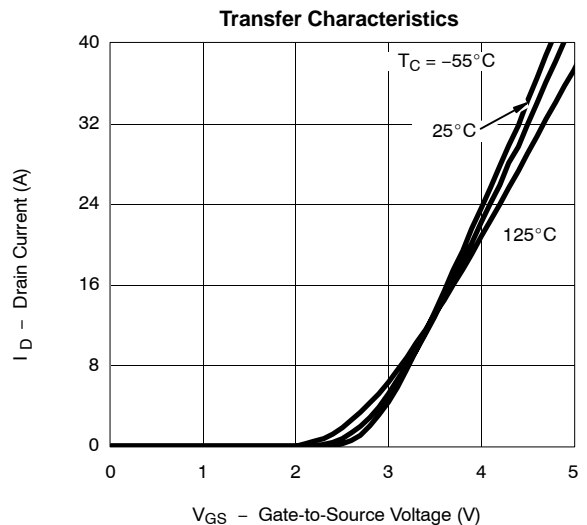
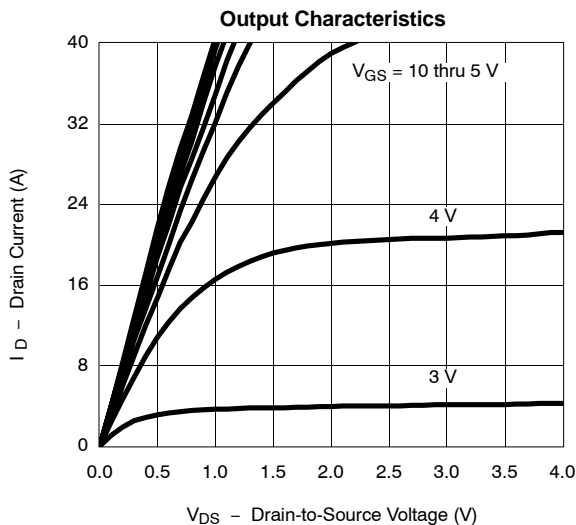
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1		-3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C			-25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -6.3 A		0.024	0.032	Ω
		V _{GS} = -4.5 V, I _D = -5.3 A		0.036	0.045	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -6.3 A		14		S
Diode Forward Voltage ^b	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -6.3 A		27	50	nC
Gate-Source Charge	Q _{gs}			6		
Gate-Drain Charge	Q _{gd}			4.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 6 Ω		16	20	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			55	80	
Fall Time	t _f			20	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.7 A, di/dt = 100 A/μs		40	90	

Notes

- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

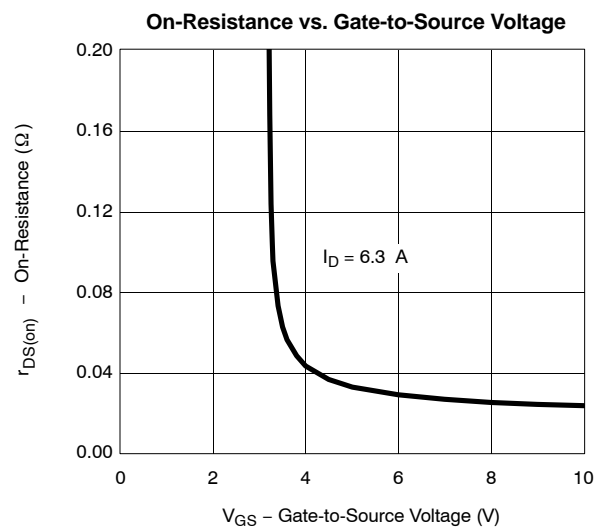
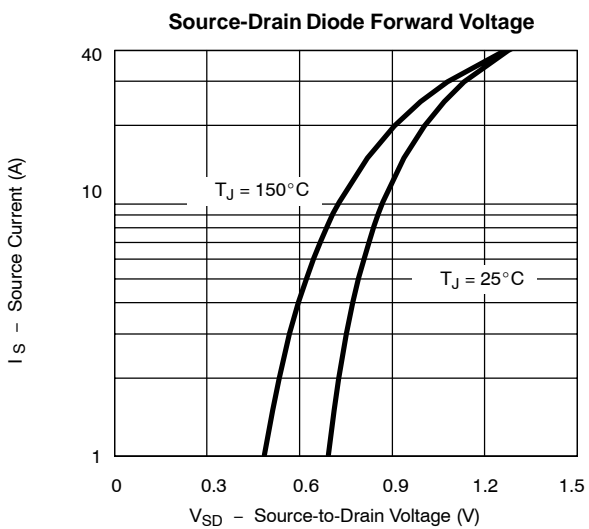
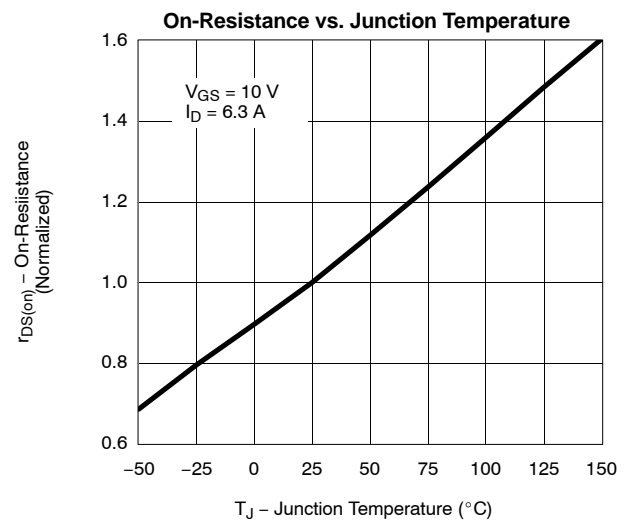
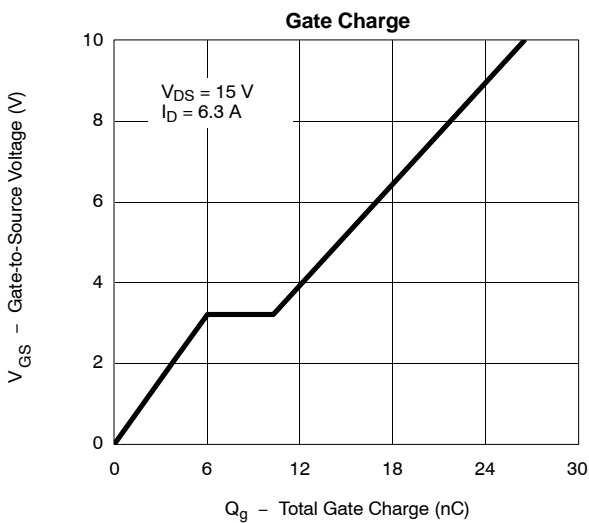
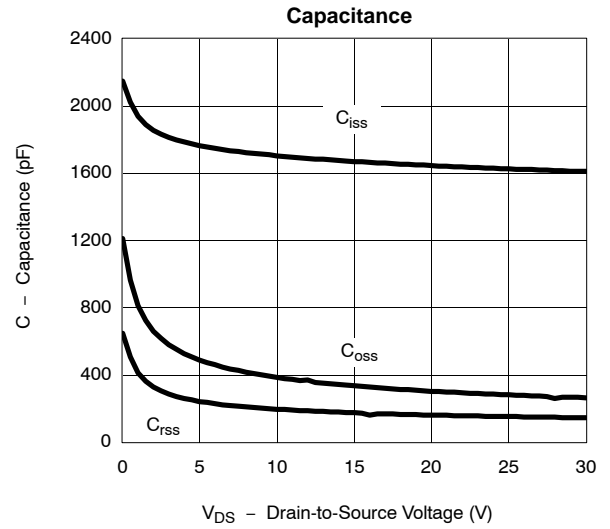
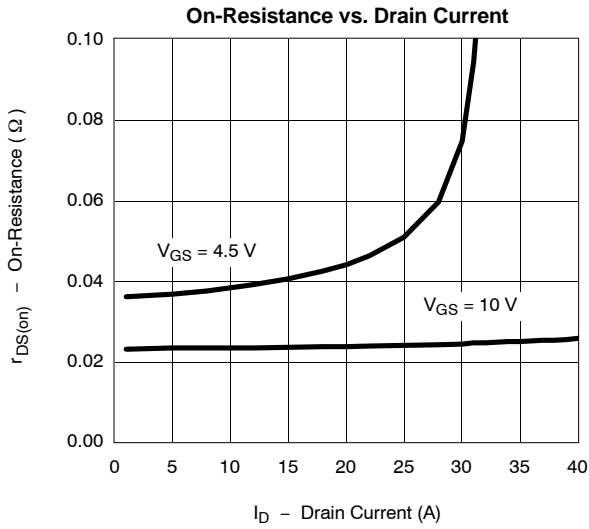
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

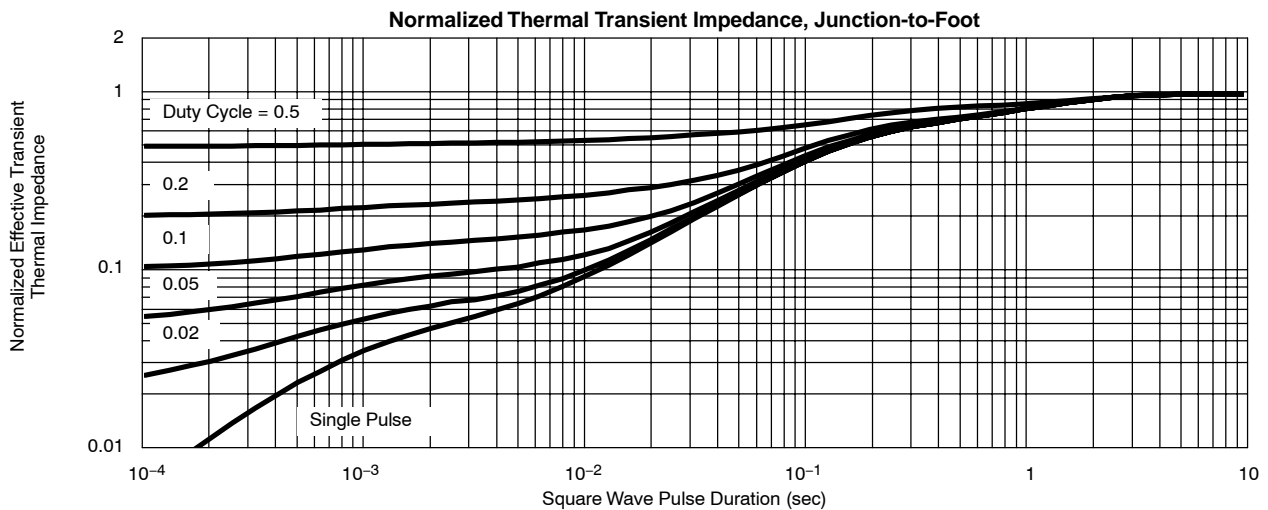
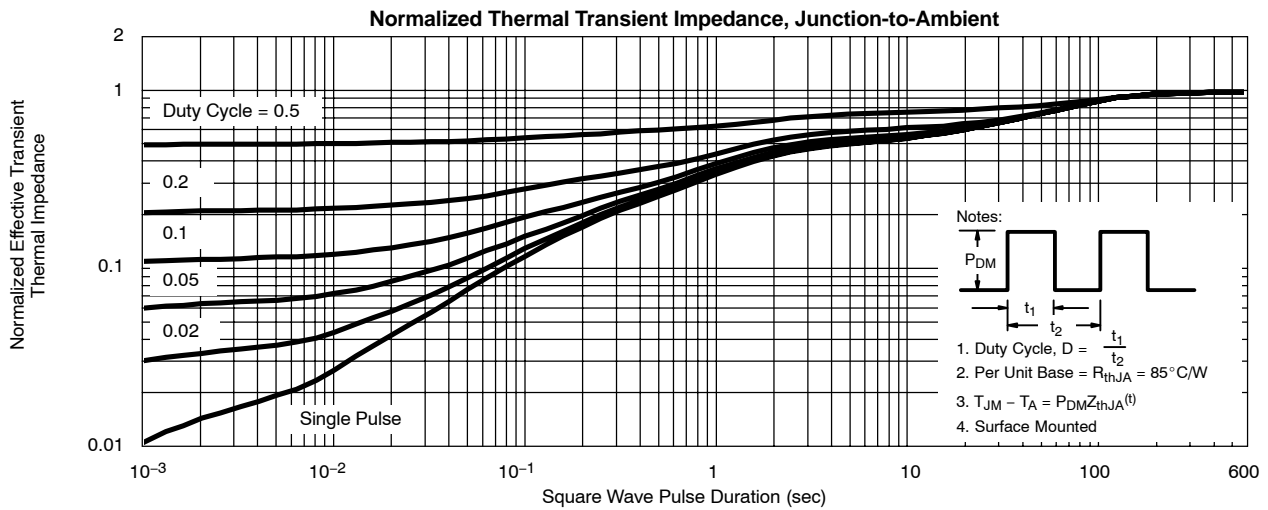
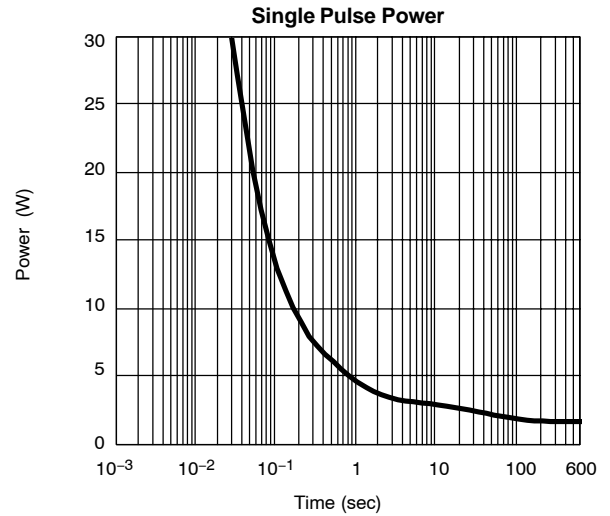
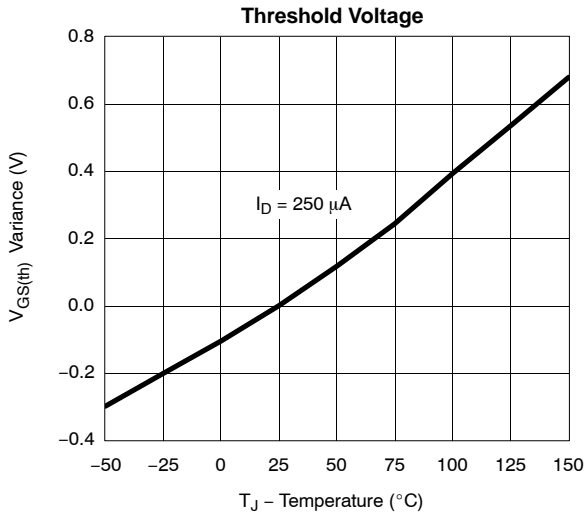




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