

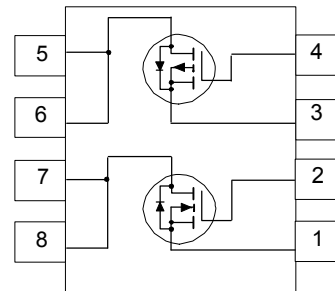
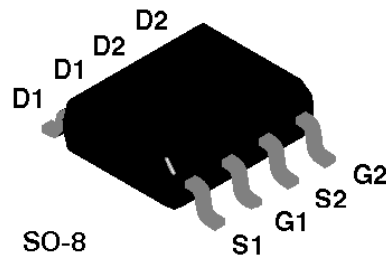
NDS9952A Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.7A, 30V, $R_{DS(ON)}=0.08\Omega$ @ $V_{GS}=10V$.
P-Channel -2.9A, -30V, $R_{DS(ON)}=0.13\Omega$ @ $V_{GS}=-10V$.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage	30	-30	V
V _{GSS}	Gate-Source Voltage	± 20	± 20	V
I _D	Drain Current - Continuous (Note 1a)	± 3.7	± 2.9	A
	- Pulsed	± 15	± 10	
P _D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to 150		°C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30			V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V <div>T_J = 55°C</div>	N-Ch			2	μA
						25	μA
		V _{DS} = -24 V, V _{GS} = 0 V <div>T_J = 55°C</div>	P-Ch			-2	μA
						-25	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	All			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA <div>T_J = 125°C</div>	N-Ch	1	1.7	2.8	V
				0.7	1.2	2.2	
		V _{DS} = V _{GS} , I _D = -250 μA <div>T_J = 125°C</div>	P-Ch	-1	-1.6	-2.8	
				-0.85	-1.25	-2.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 1.0 A <div>T_J = 125°C</div>	N-Ch		0.06	0.08	Ω
						0.08	
		V _{GS} = 4.5 V, I _D = 0.5 A <div>T_J = 125°C</div>			0.08	0.11	
					0.11	0.18	
		V _{GS} = -10 V, I _D = -1.0 A <div>T_J = 125°C</div>	P-Ch		0.11	0.13	
					0.15	0.21	
		V _{GS} = -4.5 V, I _D = -0.5 A <div>T_J = 125°C</div>			0.17	0.2	
					0.24	0.32	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	N-Ch	15			A
		V _{GS} = -10 V, V _{DS} = -5 V	P-Ch	-10			
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 3.7 A	N-Ch		6		S
		V _{DS} = -15 V, I _D = -2.9 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		320		pF
C _{oss}	Output Capacitance		P-Ch		350		
		P-Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		225		pF
P-Ch			260				
C _{rss}	Reverse Transfer Capacitance	N-Ch		85		pF	
		P-Ch		100			

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
t _{D(on)}	Turn - On Delay Time	N-Channel V _{DD} = 10 V, I _D = 1 A, V _{GEN} = 10 V, R _{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t _r	Turn - On Rise Time	P-Channel V _{DD} = -10 V, I _D = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω	N-Ch		13	20	ns
			P-Ch		21	40	
t _{D(off)}	Turn - Off Delay Time		N-Ch		21	50	ns
			P-Ch		21	90	
t _f	Turn - Off Fall Time		N-Ch		5	50	ns
			P-Ch		8	50	
Q _g	Total Gate Charge	N-Channel V _{DS} = 10 V, I _D = 3.7 A, V _{GS} = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q _{gs}	Gate-Source Charge	P-Channel V _{DS} = -10 V, I _D = -2.9 A, V _{GS} = -10 V	N-Ch		1.5		nC
			P-Ch		1.6		
Q _{gd}	Gate-Drain Charge		N-Ch		3.3		nC
			P-Ch		3.4		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.2	A
			P-Ch			-1.2	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		V _{GS} = 0 V, I _S = -1.25 A (Note 2)	P-Ch		-0.8	-1.3	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = 1.25 A, dI _F /dt = 100 A/μs	N-Ch			75	ns
		V _{GS} = 0 V, I _F = -1.25 A, dI _F /dt = 100 A/μs	P-Ch			100	

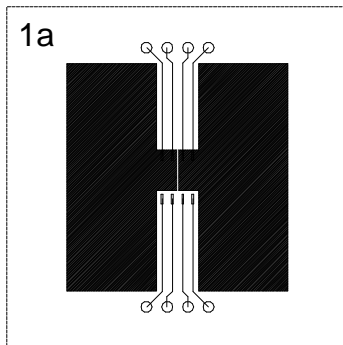
Notes:

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.

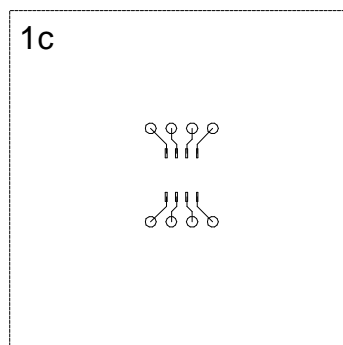
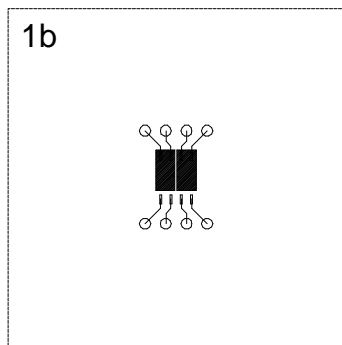
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta JA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{JA}$$

Typical R_{θJA} for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

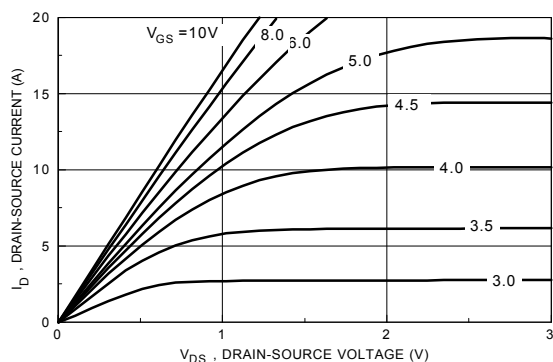


Figure 1. N-Channel On-Region Characteristics.

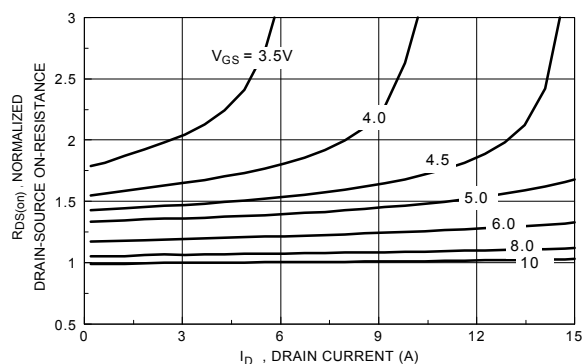


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

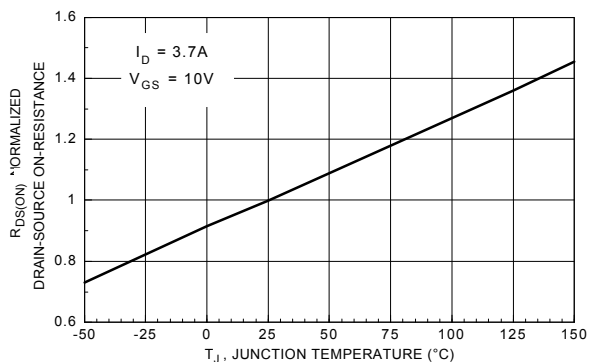


Figure 3. N-Channel On-Resistance Variation with Temperature.

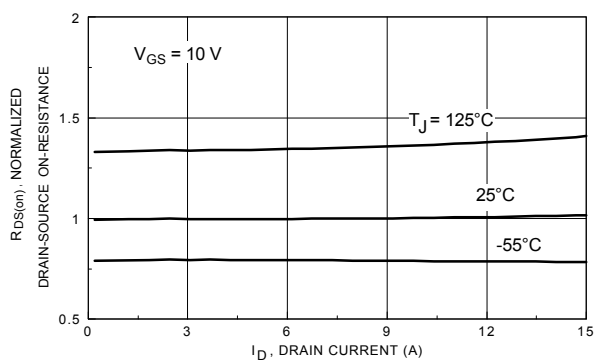


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

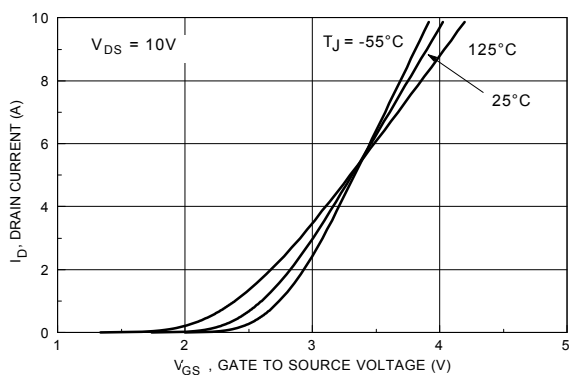


Figure 5. N-Channel Transfer Characteristics.

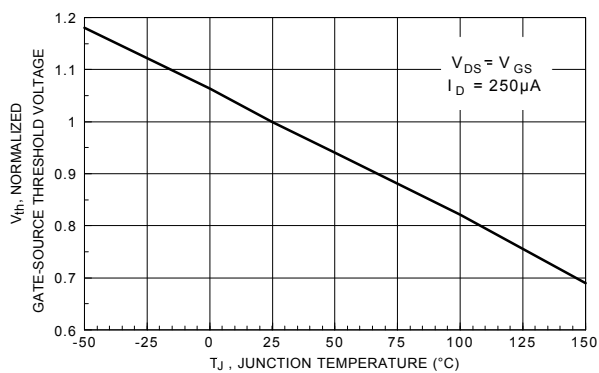


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

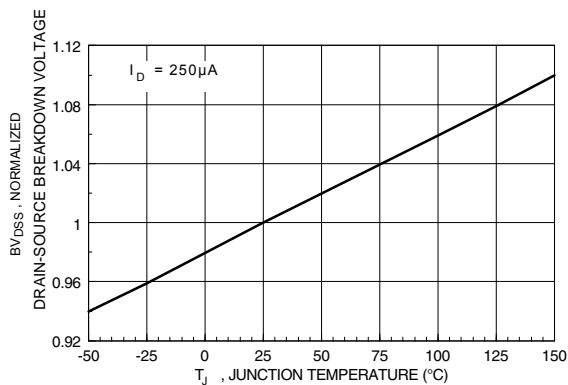


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

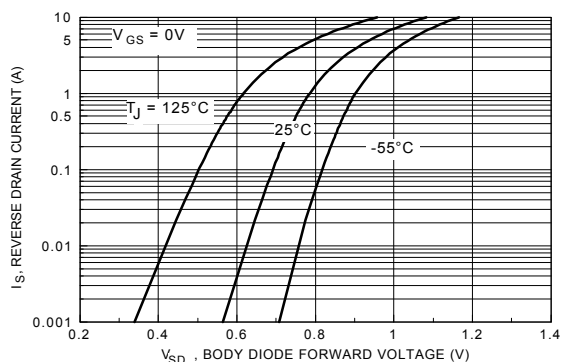


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

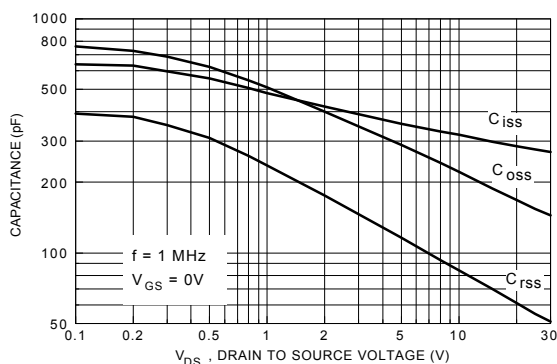


Figure 9. N-Channel Capacitance Characteristics.

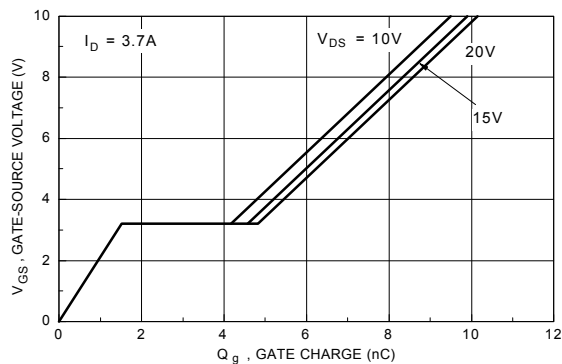


Figure 10. N-Channel Gate Charge Characteristics.

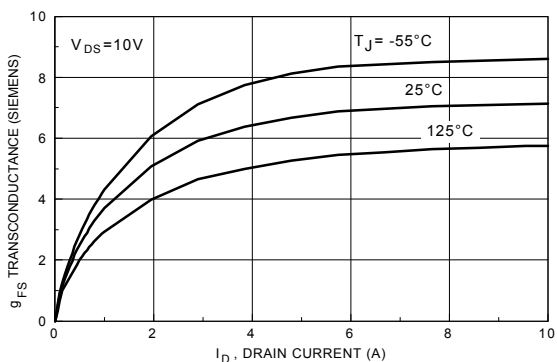


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

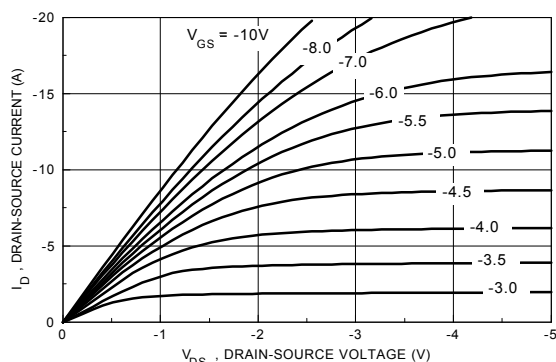


Figure 12. P-Channel On-Region Characteristics.

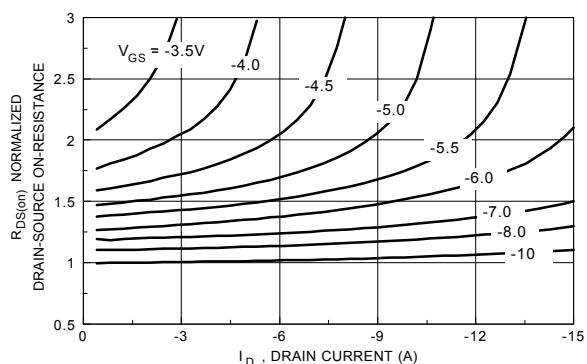


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

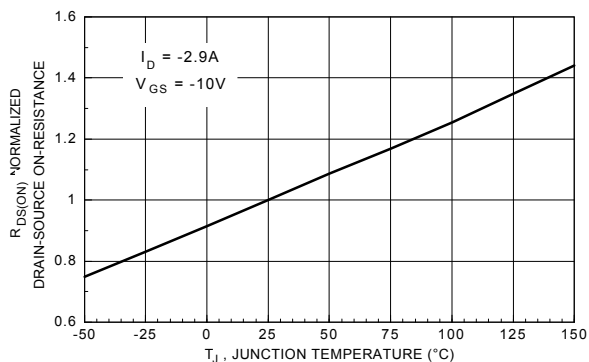


Figure 14. P-Channel On-Resistance Variation with Temperature.

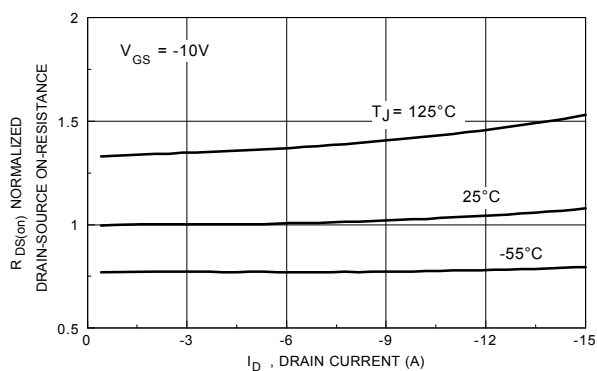


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

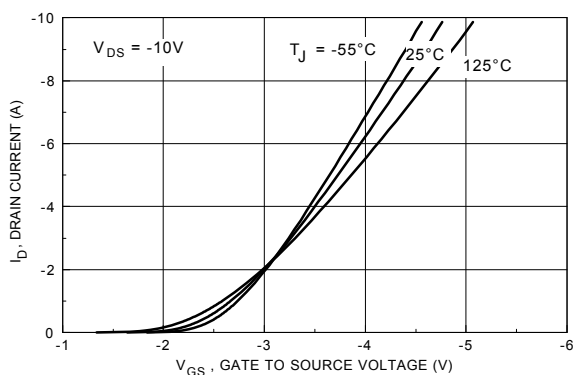


Figure 16. P-Channel Transfer Characteristics.

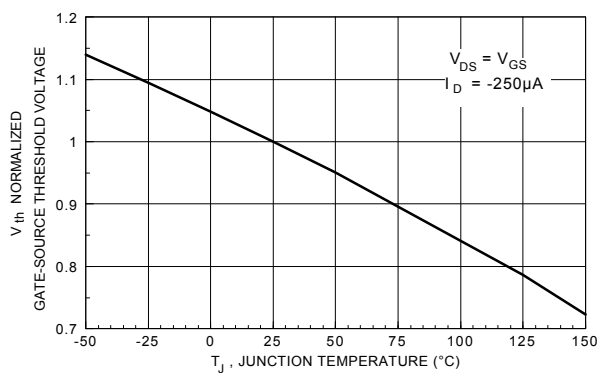


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

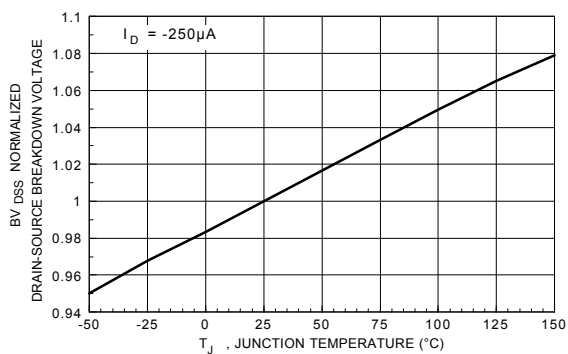


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

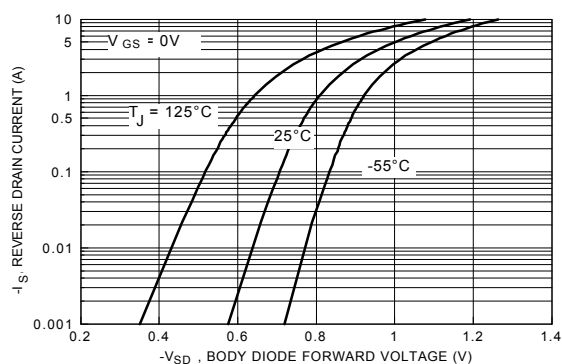


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

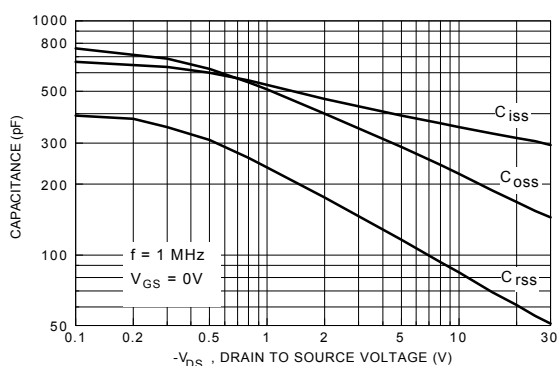


Figure 20. P-Channel Capacitance Characteristics.

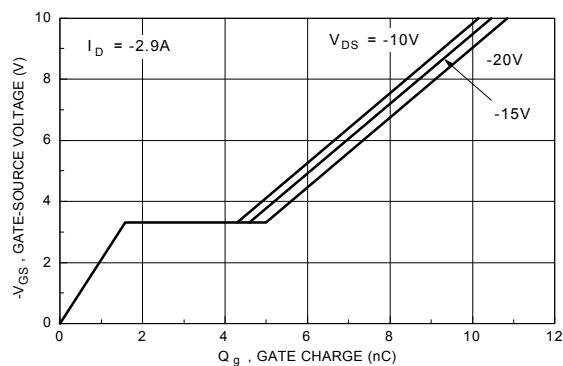


Figure 21. P-Channel Gate Charge Characteristics.

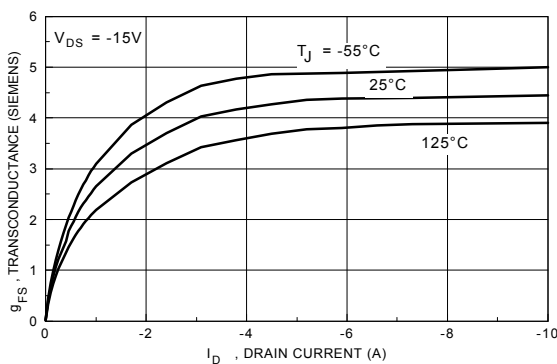


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

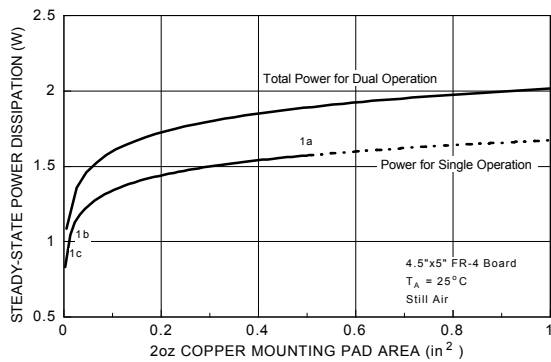


Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

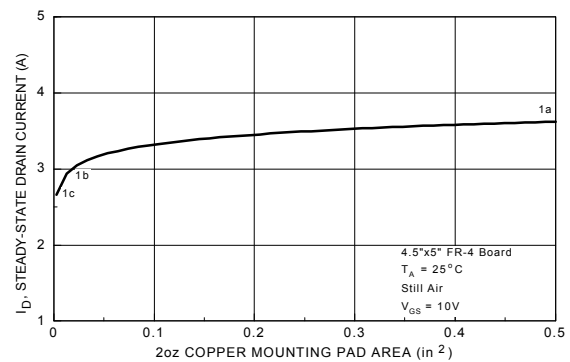


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

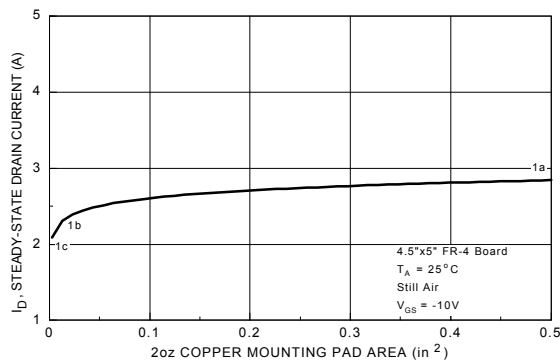


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

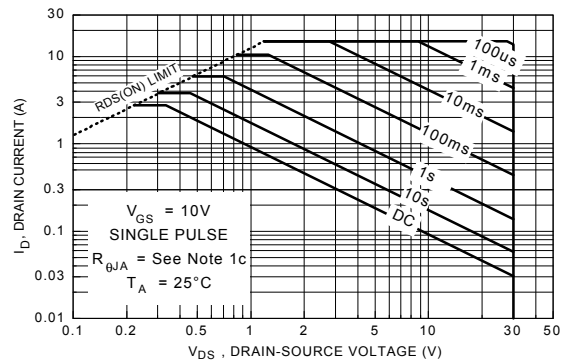


Figure 26. N-Channel Maximum Safe Operating Area.

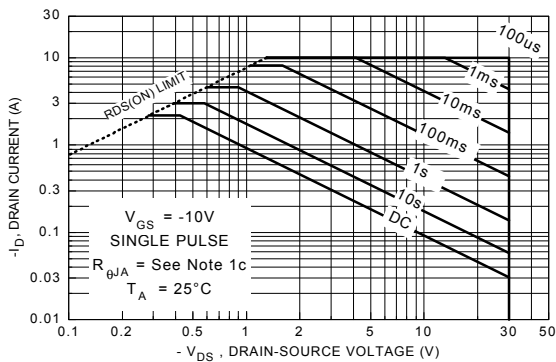


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

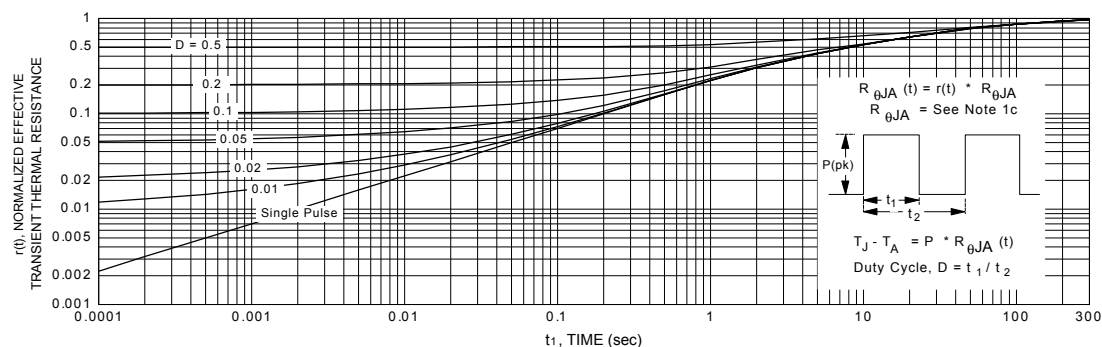


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

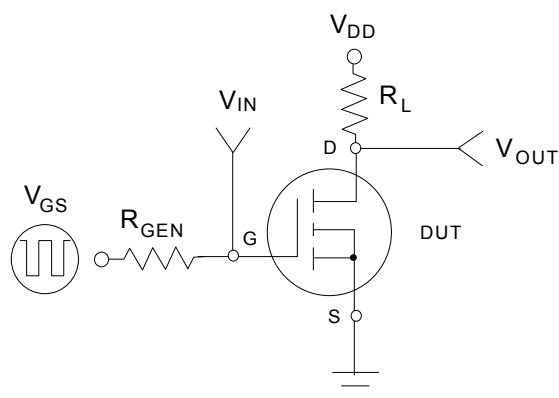


Figure 29. N or P-Channel Switching Test Circuit.

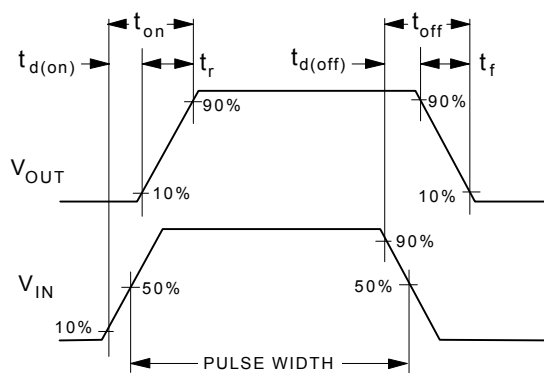
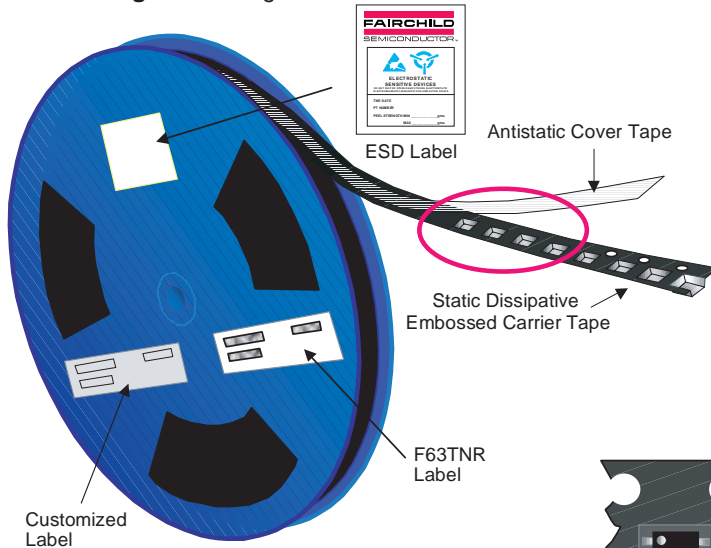


Figure 30. N or P-Channel Switching Waveforms.

SO-8 Tape and Reel Data and Package Dimensions



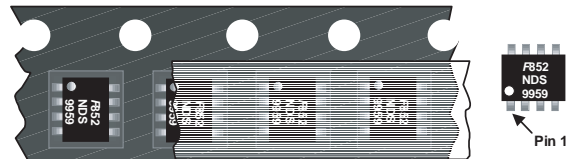
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

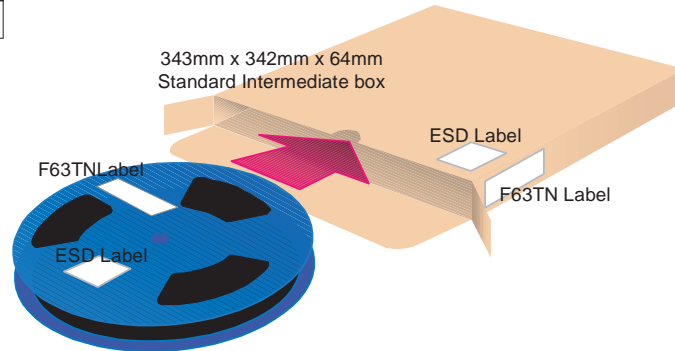
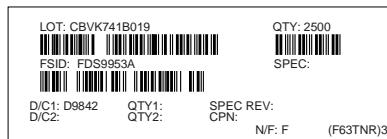
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



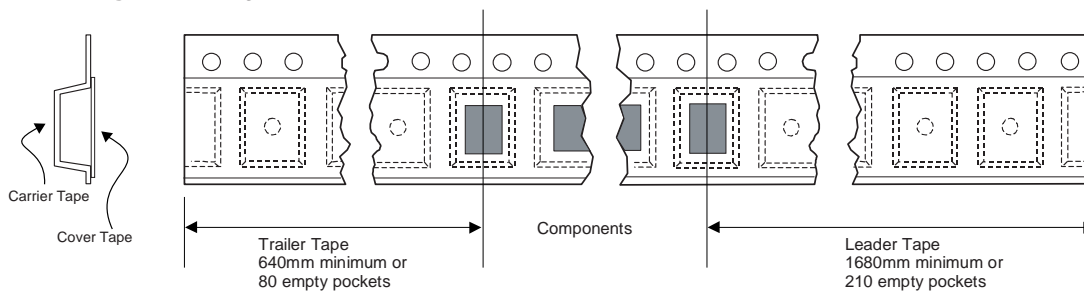
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample

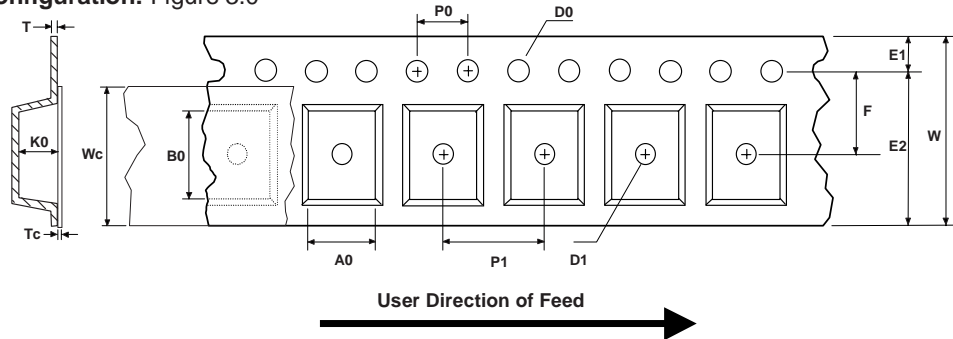


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



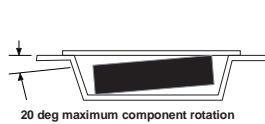
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

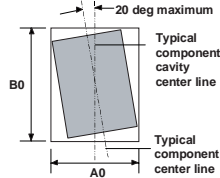


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

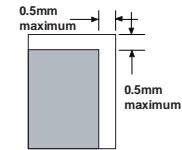
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

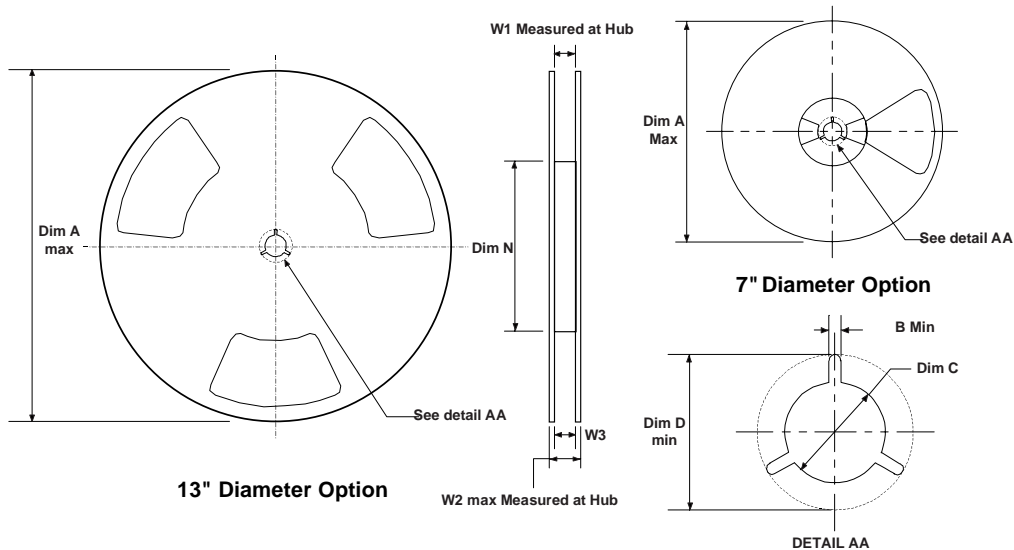


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

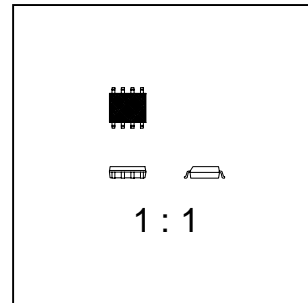
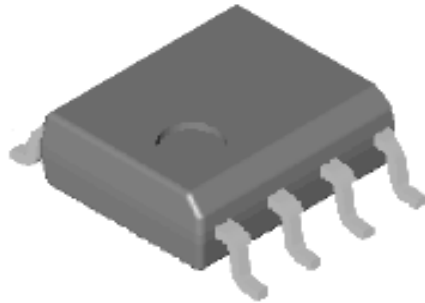
SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

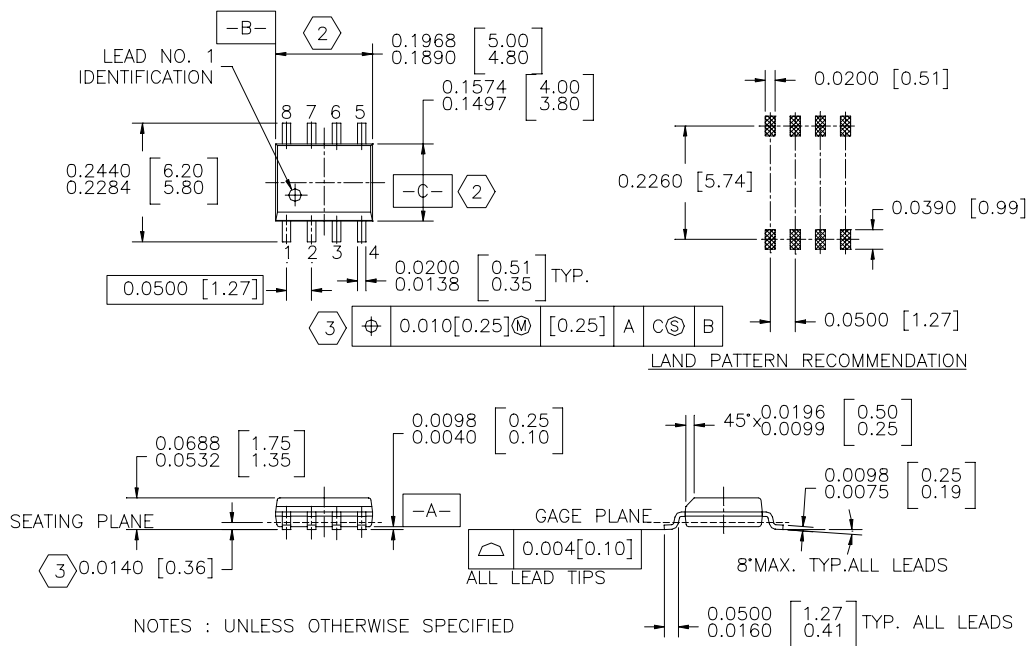
SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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