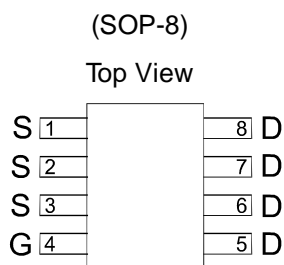


P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4435 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION



Ordering Information: ME4435 (Pb-free)

ME4435-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	TA=25°C	-8.8
		TA=70°C	-7.1
Pulsed Drain Current	I _{DM}	-35	A
Maximum Power Dissipation	P _D	TA=25°C	2.5
		TA=70°C	1.6
Operating Junction Temperature	T _J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	R _{θJA}	50	°C/W

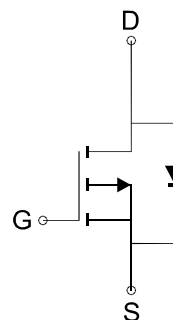
*The device mounted on 1in² FR4 board with 2 oz copper

FEATURES

- R_{DS(ON)} ≤ 20mΩ@V_{GS}=-10V
- R_{DS(ON)} ≤ 35mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET



P-Channel 30V (D-S) MOSFET
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1	-1.4	-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
I _{D(ON)}	On-State Drain Current ^a	V _{DS} =-5V, V _{GS} =-10V	-30			A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D =-9.1A		15	20	mΩ
		V _{GS} =-4.5V, I _D =-6.9A		25	35	
V _{SD}	Diode Forward Voltage	I _S =-2.1A, V _{GS} =0V		-0.8	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-9.1A		38		nC
Q _{gs}	Gate-Source Charge			7.7		
Q _{gd}	Gate-Drain Charge			9		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		6.9		Ω
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		1490		pF
C _{oss}	Output Capacitance			209		
C _{rss}	Reverse Transfer Capacitance			148		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1A, V _{GEN} =-10V R _G =6Ω		38.2		ns
t _r	Turn-On Rise Time			16.7		
t _{d(off)}	Turn-Off Delay Time			106		
t _f	Turn-Off Fall Time			24.1		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

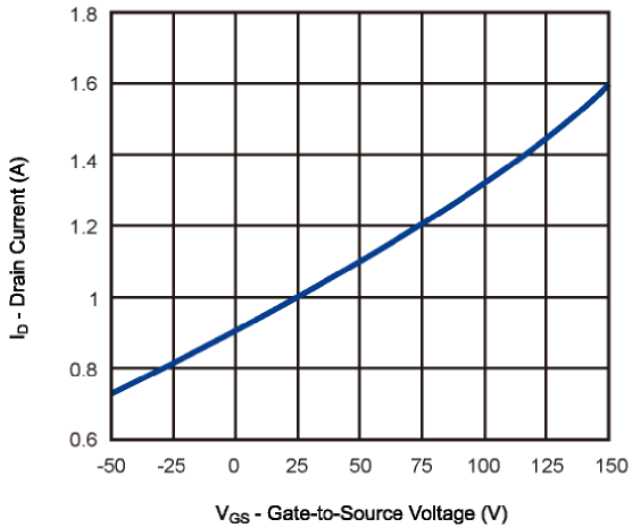
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

DCC
正式發行

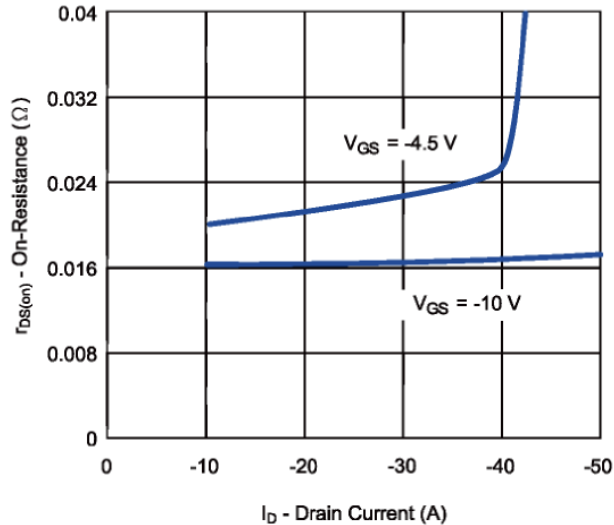
P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

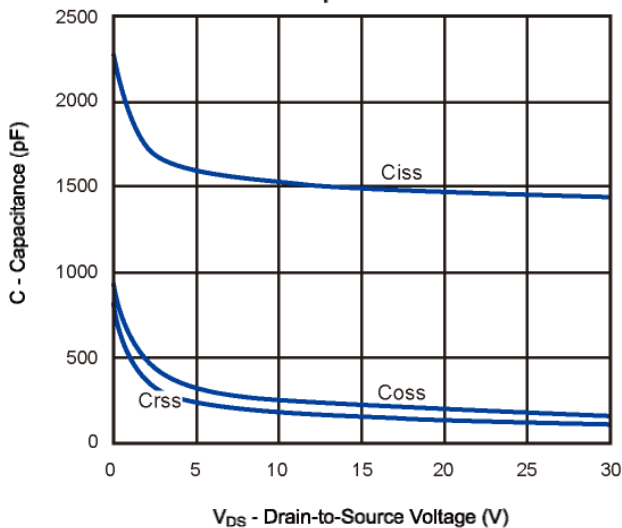
Transfer Characteristics



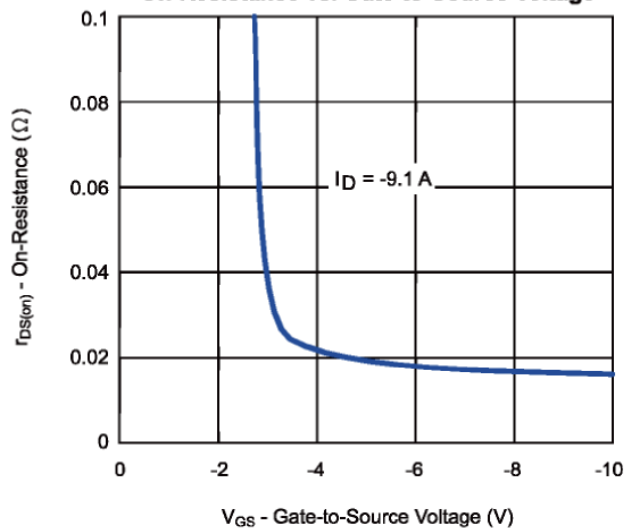
On-Resistance vs. Drain Current



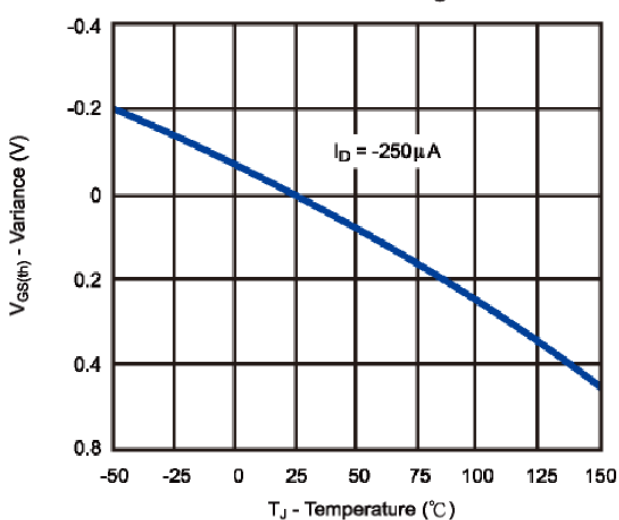
Capacitance



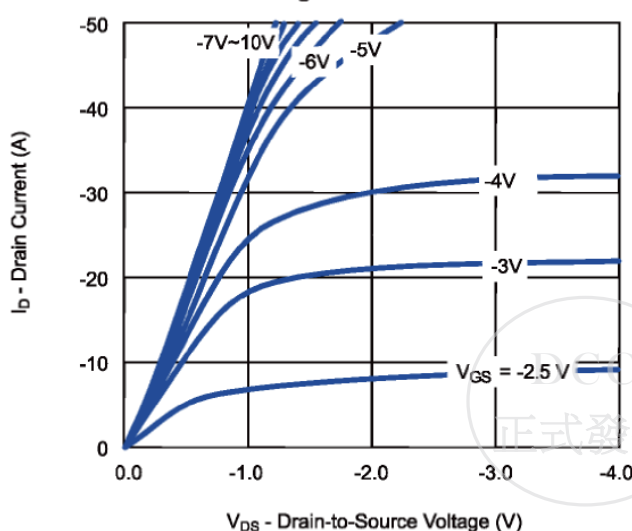
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

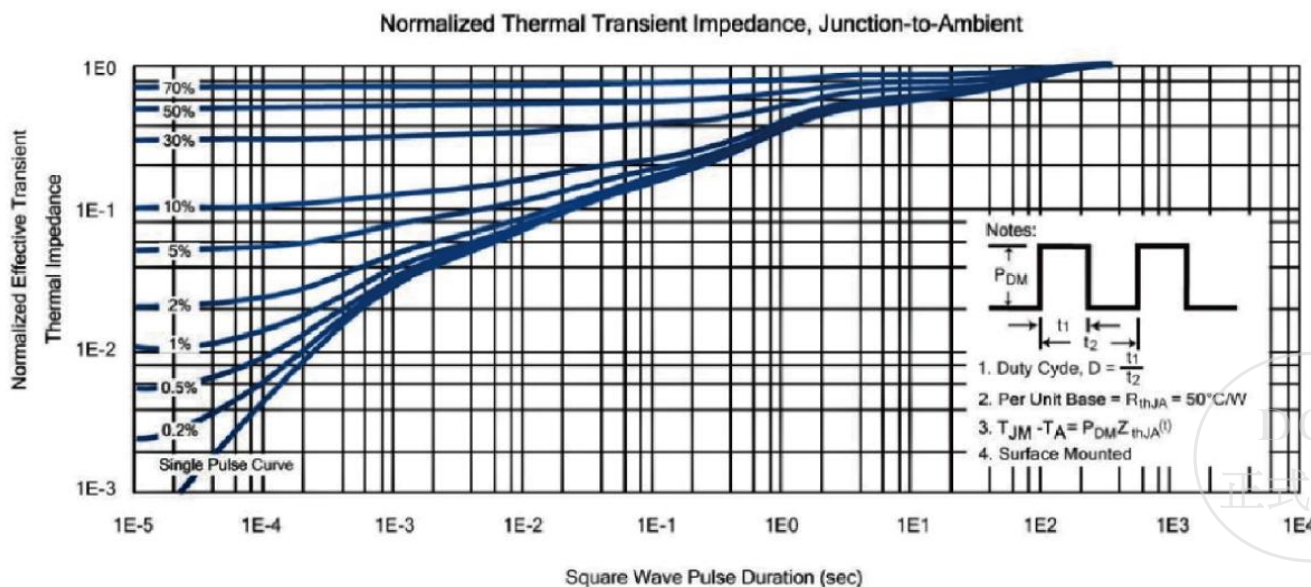
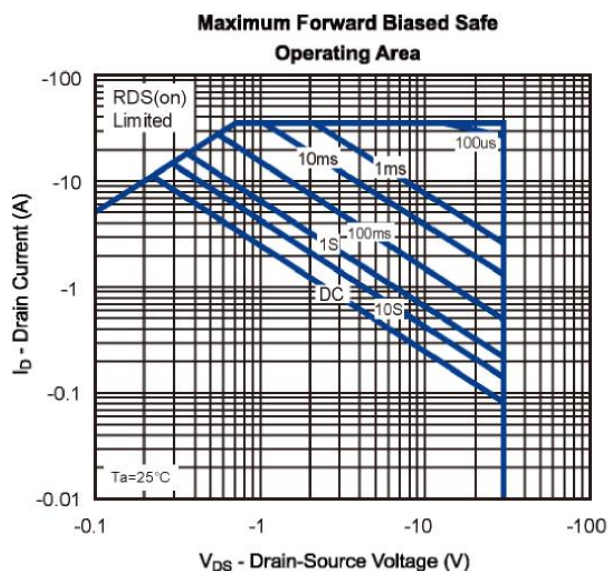
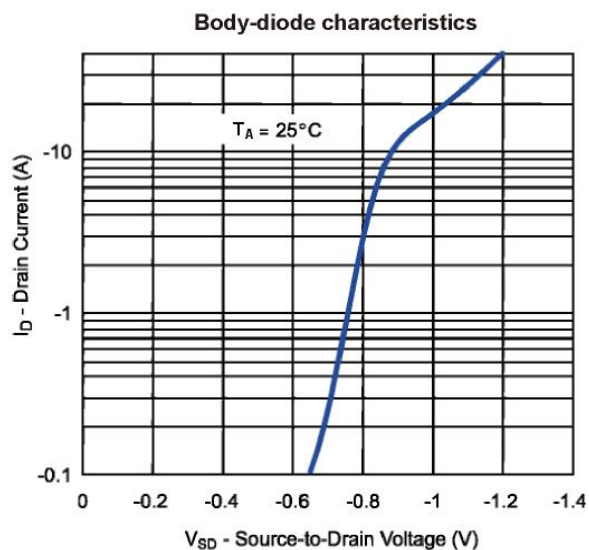
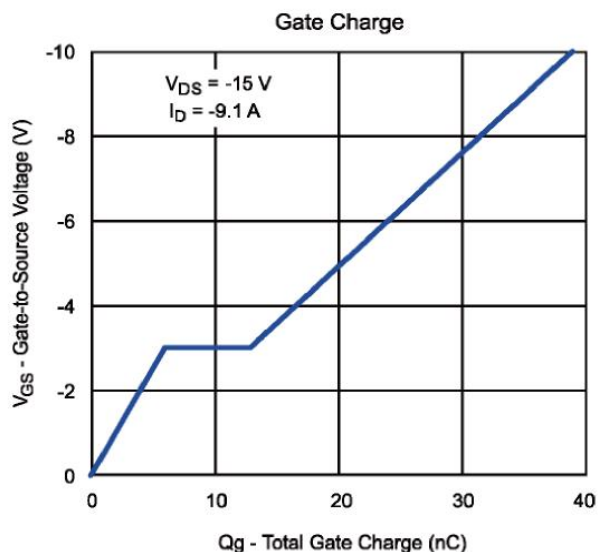


On-Region Characteristics

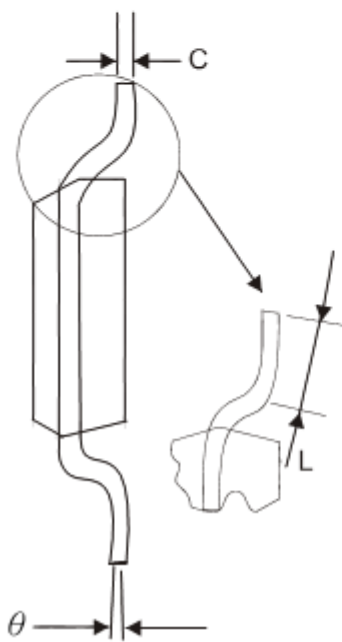
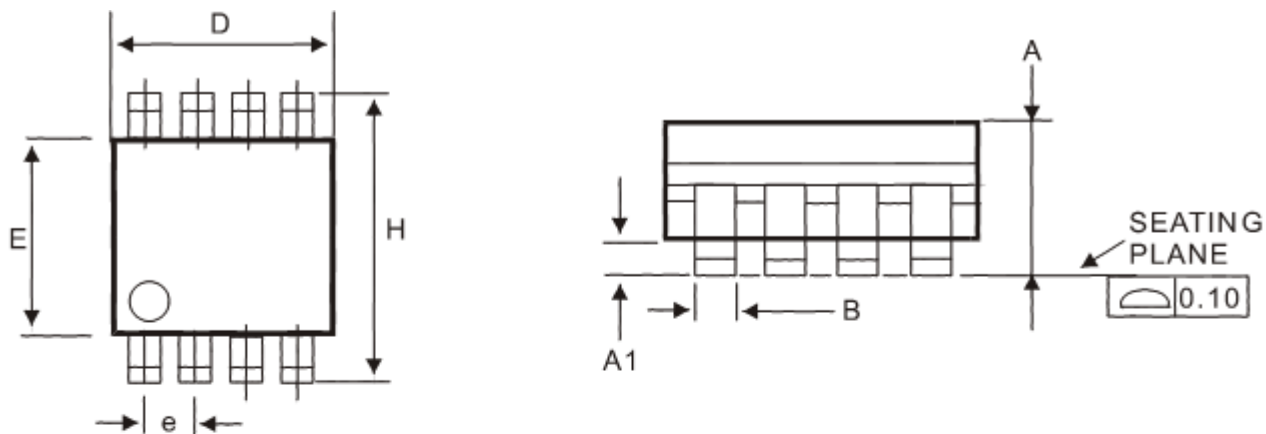


P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

