

FDS6912A

Dual N-Channel, Logic Level, PowerTrench™ MOSFET

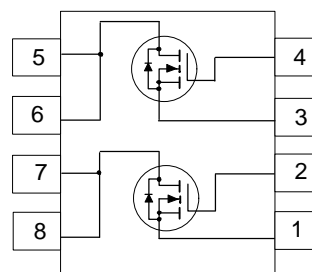
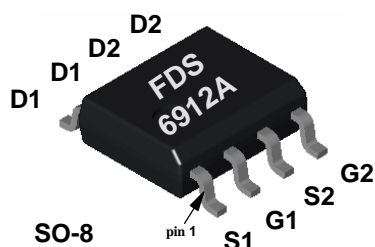
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 6 A, 30 V. $R_{DS(ON)} = 0.028 \Omega$ @ $V_{GS} = 10$ V
 $R_{DS(ON)} = 0.035 \Omega$ @ $V_{GS} = 4.5$ V.
- Fast switching speed.
- Low gate charge (typical 9 nC).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDS6912A	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	6	A
	- Pulsed	20	
P_D	Power Dissipation for Single Operation (Note 1a)	2	W
	(Note 1b)	1.6	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

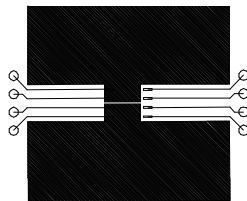
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

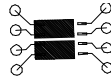
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		23		mV / °C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		T _J = 55°C			10	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.5	3	V
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		-4		mV / °C
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 6 A		0.023	0.028	Ω
		T _J = 125°C		0.036	0.044	
		V _{GS} = 4.5 V, I _D = 5 A		0.029	0.035	
I _{D(ON)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	20			A
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 6 A		18		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		830		pF
C _{oss}	Output Capacitance			185		pF
C _{rss}	Reverse Transfer Capacitance			80		pF
SWITCHING CHARACTERISTICS (Note 2)						
t _{D(on)}	Turn - On Delay Time	V _{DS} = 15 V, I _D = 1 A		6	12	ns
t _r	Turn - On Rise Time	V _{GS} = 10 V, R _{GEN} = 6 Ω		10	18	ns
t _{D(off)}	Turn - Off Delay Time			18	29	ns
t _f	Turn - Off Fall Time			5	12	ns
Q _g	Total Gate Charge	V _{DS} = 15 V, I _D = 7.5 A,		9	13	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V		2.8		nC
Q _{gd}	Gate-Drain Charge			3.1		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)		0.73	1.2	V

Notes:

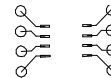
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

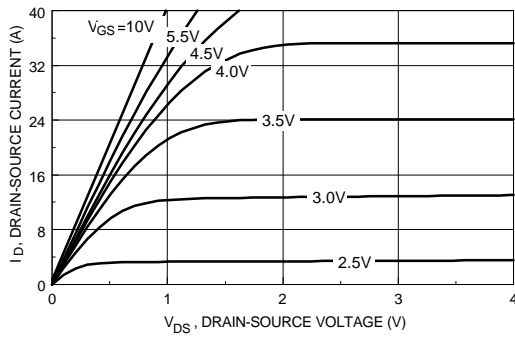


Figure 1. On-Region Characteristics.

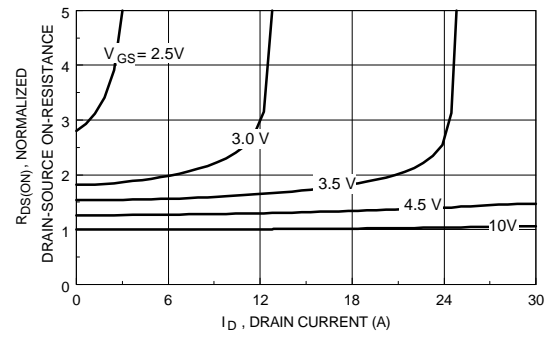


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

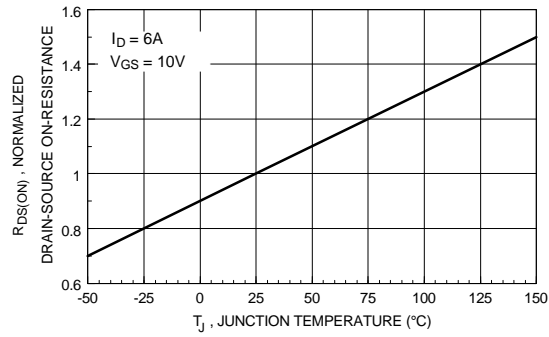


Figure 3. On-Resistance Variation with Temperature.

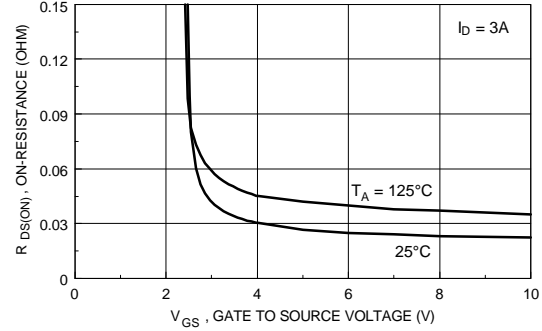


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

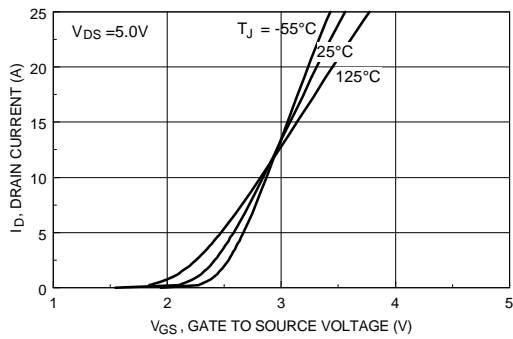


Figure 5. Transfer Characteristics.

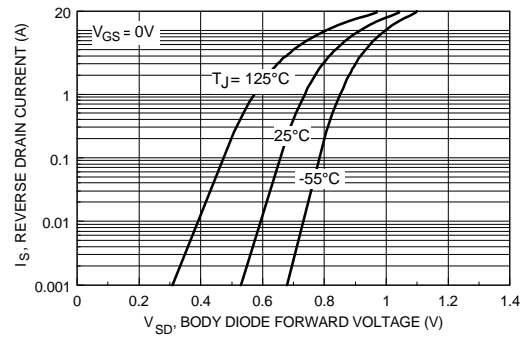


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics

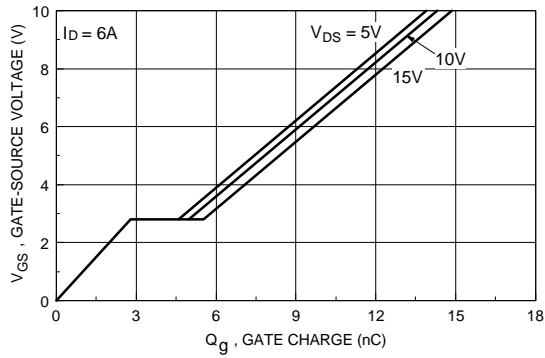


Figure 7. Gate Charge Characteristics.

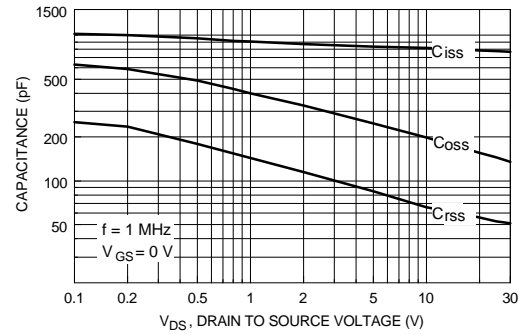


Figure 8. Capacitance Characteristics.

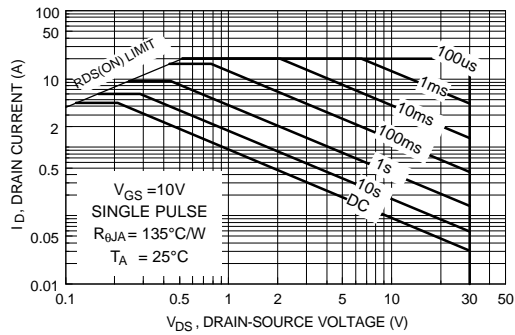


Figure 9. Maximum Safe Operating Area.

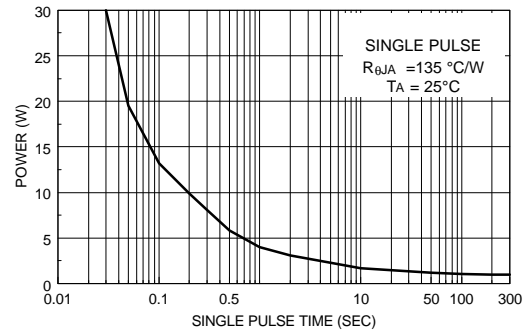


Figure 10. Single Pulse Maximum Power Dissipation.

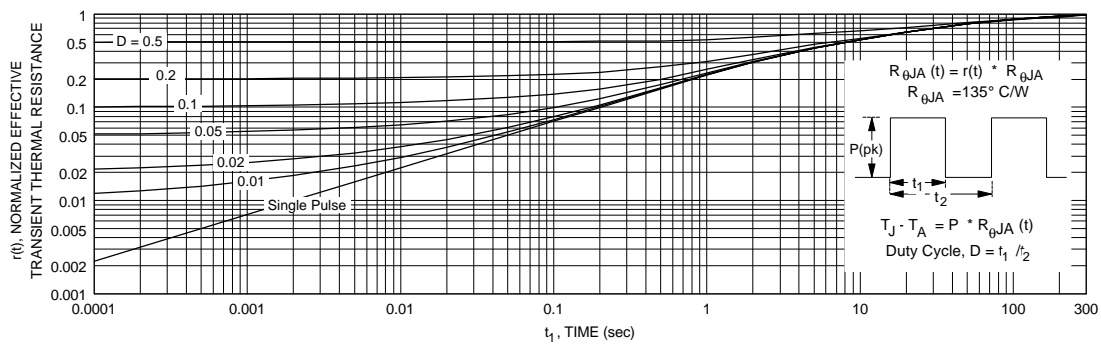


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.
Transient thermal response will change depending on the circuit board design.