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## FDL100N50F N-Channel UniFET<sup>TM</sup> FRFET<sup>®</sup> MOSFET **500 V, 100 A, 55 m**Ω

### **Features**

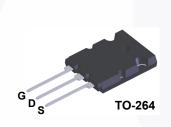
- $R_{DS(on)}$  = 43 m $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 50 A
- Low Gate Charge (Typ. 238 nC)
- Low C<sub>rss</sub> (Typ. 64 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

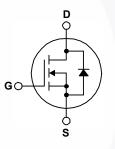
### Applications

- · Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FDL100N50F	Unit		
V <sub>DSS</sub>	Drain to Source Voltage			500	V	
V <sub>GSS</sub>	Gate to Source Voltage			±30	V	
ID	Drain Current	- Continuous (T <sub>C</sub> = 25 <sup>o</sup> C)		100		
		- Continuous (T <sub>C</sub> = 100 <sup>o</sup> C)		60	A	
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	400	Α	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)			5000	mJ	
I <sub>AR</sub>	Avalanche Current (Note 1)			100	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		73.5	mJ		
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	20	V/ns	
P <sub>D</sub>	Dewer Dissinction	(T <sub>C</sub> = 25 <sup>o</sup> C)		2500	W	
	Power Dissipation	- Derate Above 25°C		20	W/ºC	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +150	°C	
T <sub>I</sub>	Maximum Lead Temperate	ure for Soldering, 1/8" from Case for 5 Se	conds	300	°C	

### **Thermal Characteristics**

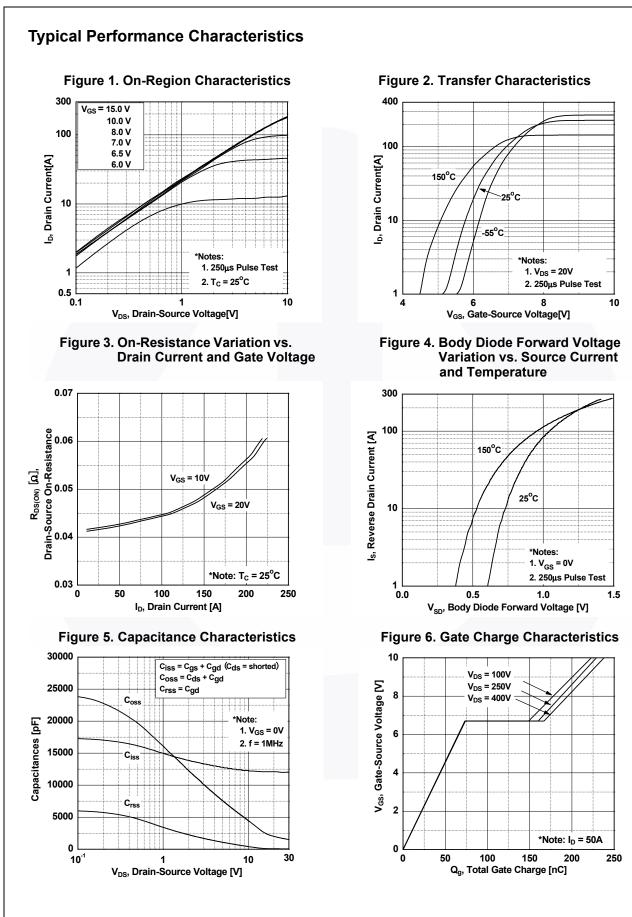
Symbol	Parameter	FDL100N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.05	°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	30	°C/vv

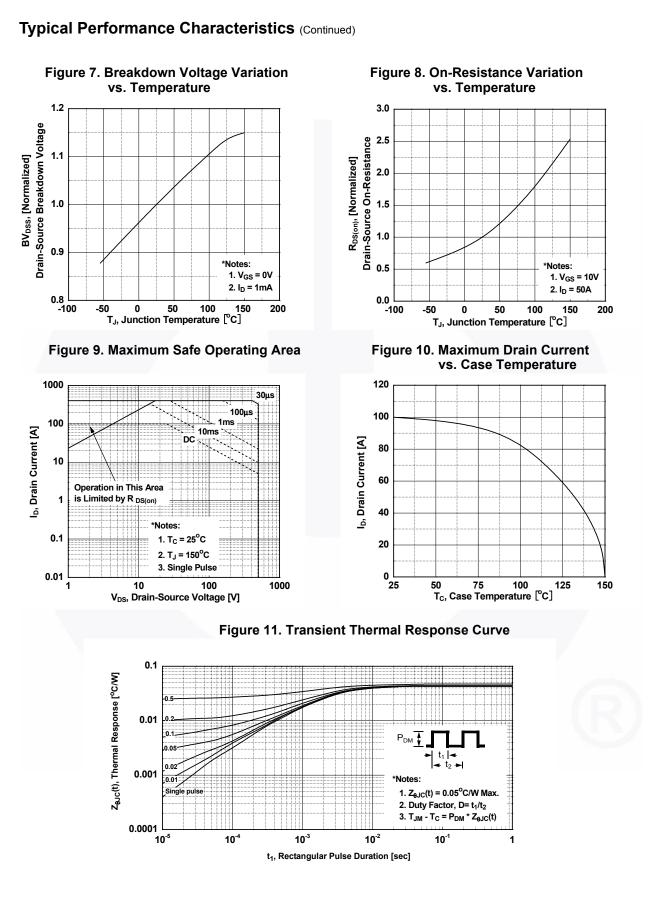
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### November 2013

	Part Number Top Mark		Package	Packing Method	Reel Size	e Ta	ape Width	Qua	antity	
FDL100			TO-264	Tube	N/A		N/A	25	25 units	
Electrica	l Chara	acteristics T <sub>C</sub> = 25°C u	unless othe	rwise noted.				·		
Symbol		Parameter		Test Condition	S	Min.	Тур.	Max.	Unit	
Off Charac	toristics									
	1		- II -	- 250 A \/ 0 \/	- 25 <sup>0</sup> C	500	_	-	V	
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage			$I_D = 250 \ \mu\text{A}, \ V_{GS} = 0 \ V, \ T_C = 25^{\circ}\text{C}$		500	-	-	V	
$\Delta BV_{DSS}$ Breakd / $\Delta T_J$ Coeffic		akdown Voltage Temperature		$I_D = 250 \ \mu A$ , Referenced to $25^{\circ}C$		-	0.5	-	V/ºC	
7 Δ1			Vn	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	10	μA	
IDSS	Zero Gat	Zero Gate Voltage Drain Current		<sub>S</sub> = 400 V, T <sub>C</sub> = 125°C		-	-	100		
I <sub>GSS</sub>	Gate to E	Body Leakage Current		<sub>S</sub> = ±30 V, V <sub>DS</sub> = 0 V		-	-	±100	nA	
On Charac	teristics									
V <sub>GS(th)</sub>		reshold Voltage	Va	<sub>S</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA		3.0	_	5.0	V	
R <sub>DS(on)</sub>		ain to Source On Resistance	-	$s = v_{DS}, r_{D} = 200 \mu A$ $s = 10  V, r_{D} = 50  A$		-	0.043	0.055	Ω	
9FS		Transconductance	-	$_{\rm S}$ = 20 V, I <sub>D</sub> = 50 A		-	95	-	S	
95	1 or Ward	Trancoortiductarioo	•U	5 20 0, 10 00 / 1					0	
Dynamic C	Characte	ristics								
C <sub>iss</sub>	Input Ca	pacitance		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		-	12000	-	pF	
C <sub>oss</sub>	Output C	Capacitance				-	1700	-	pF	
C <sub>rss</sub>	Reverse	Transfer Capacitance				-	64	-	pF	
Q <sub>g(tot)</sub>	Total Gat	te Charge at 10V	Vn	<sub>D</sub> = 400 V, I <sub>D</sub> = 50 A,		-	238	-	nC	
Q <sub>gs</sub>	Gate to S	Source Gate Charge		$V_{GS} = 10 V$ (Note 4)		-	74	-	nC	
Q <sub>gd</sub>	Gate to I	Drain "Miller" Charge				-	95	-	nC	
Switching	Charact	eristics								
t <sub>d(on)</sub>		Delay Time				-	63	-	ns	
t <sub>r</sub>		Rise Time		$_{\rm D}$ = 250 V, $I_{\rm D}$ = 50 A, $_{\rm S}$ = 10 V, $R_{\rm G}$ = 4.7 $\Omega$		-	186	-	ns	
t <sub>d(off)</sub>		Delay Time	↓G	S = 10 V, ICG = 4.7 S2		-	202	-	ns	
t <sub>f</sub>		Fall Time		(Note 4)			105	-	ns	
	rce Diod	e Characteristics			1			1	1	
		n Continuous Drain to Source	a Diode Fo	nward Current			_	100	Α	
ls lou		n Pulsed Drain to Source Dio					-	400	A	
V <sub>SD</sub>		Source Diode Forward Voltage		<sub>S</sub> = 0 V, I <sub>SD</sub> = 100 A	1	-	-	1.5	V	
		Recovery Time				-	250	-	ns	
		Recovery Charge		V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 100 A dI <sub>E</sub> /dt = 100 A/μs		-	1.5	-	uC	
t <sub>rr</sub> Q <sub>rr</sub>								1		

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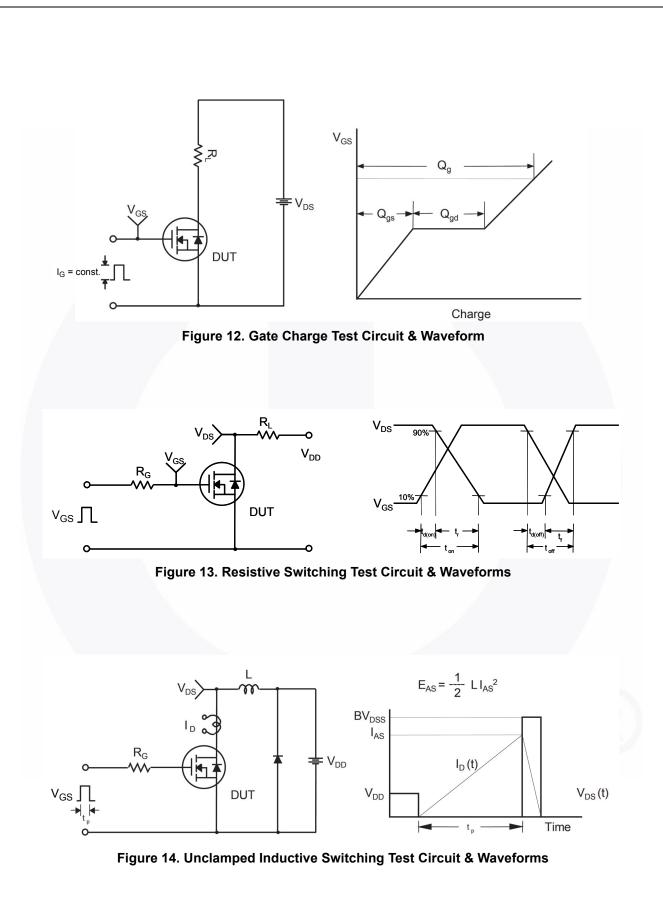




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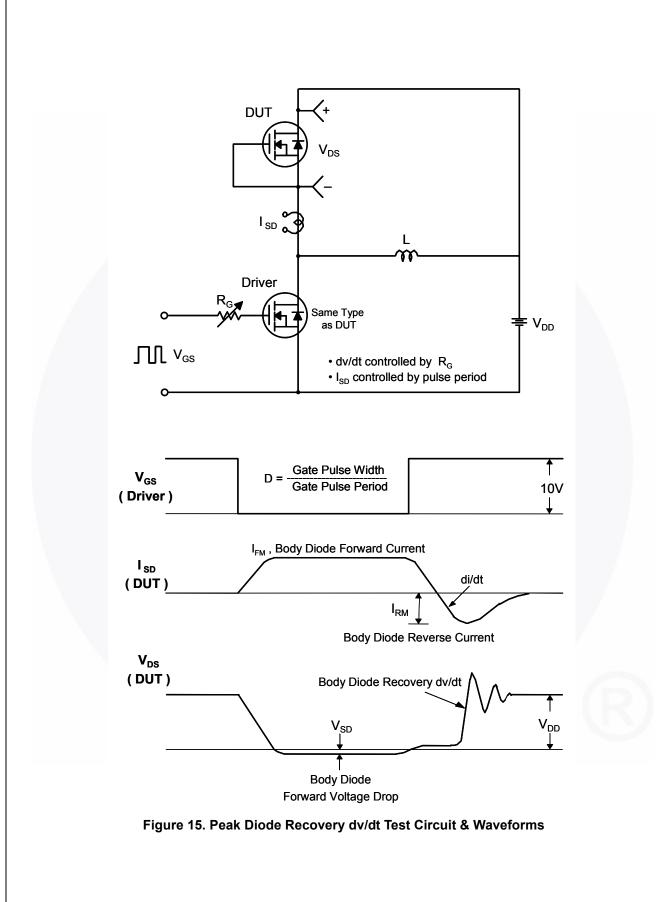
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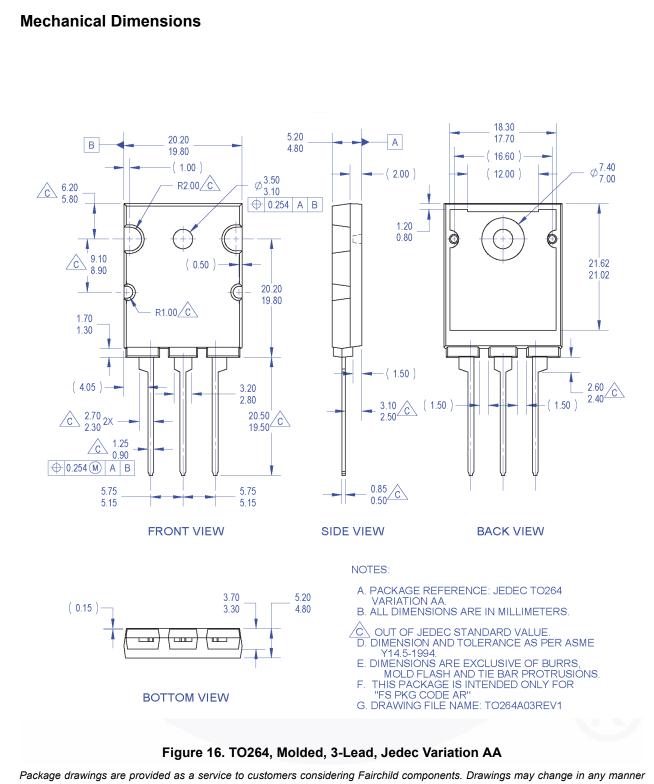
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5





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