

FDC6506P

Dual P-Channel Logic Level PowerTrench™ MOSFET

General Description

These P-Channel logic level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

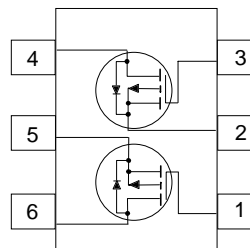
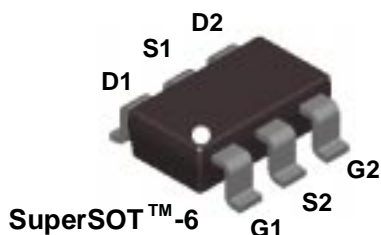
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

Applications

- Load switch
- Battery protection
- Power management

Features

- -1.8 A, -30 V. $R_{DS(on)} = 0.170 \Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(on)} = 0.280 \Omega @ V_{GS} = -4.5 \text{ V}$
- Low gate charge (2.3nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a) - Pulsed	-1.8	A
		-10	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96	W
		0.9	
		0.7	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ\text{C/W}$

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.506	FDC6506P	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		-20		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.8\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -1.8\text{ A}$ @ 125°C $V_{GS} = -4.5\text{ V}, I_D = -1.4\text{ A}$		0.14 0.20 0.22	0.17 0.27 0.28	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-10			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -1.8\text{ A}$		3		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		190		pF
C_{oss}	Output Capacitance			70		pF
C_{rss}	Reverse Transfer Capacitance			30		pF

Switching Characteristics (Note 2)

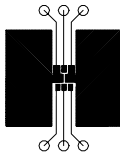
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		7	14	ns
t_r	Turn-On Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
t_f	Turn-Off Fall Time			2	6	ns
Q_g	Total Gate Charge	$V_{DS} = -5\text{ V}, I_D = -1.8\text{ A},$ $V_{GS} = -10\text{ V}$		2.3	3.5	nC
Q_{gs}	Gate-Source Charge			1		nC
Q_{gd}	Gate-Drain Charge			0.8		nC

Drain-Source Diode Characteristics and Maximum Ratings

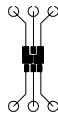
I _S	Maximum Continuous Drain-Source Diode Forward Current				-0.8	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.8 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) $130\text{ }^\circ\text{C/W}$ when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) $140\text{ }^\circ\text{C/W}$ when mounted on a 0.005 in^2 pad of 2 oz. copper.



c) $180\text{ }^\circ\text{C/W}$ when mounted on a 0.0015 in^2 pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

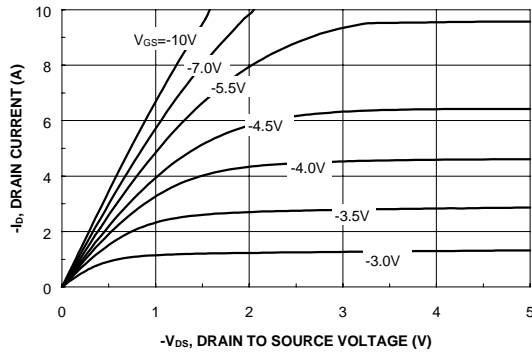


Figure 1. On-Region Characteristics.

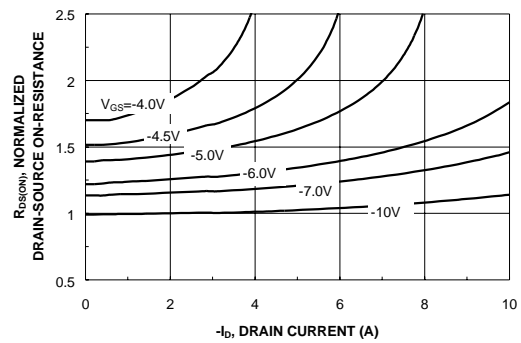


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

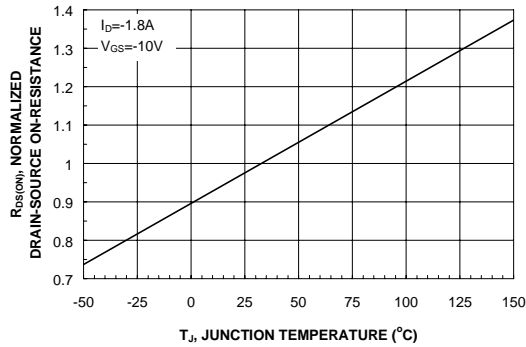


Figure 3. On-Resistance Variation with Temperature.

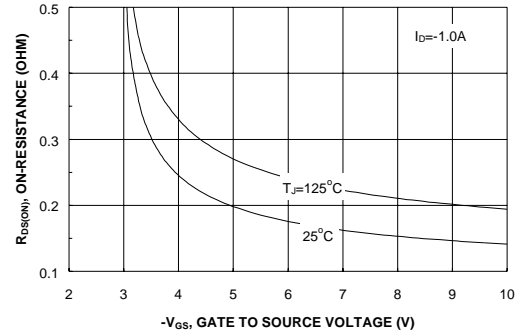


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

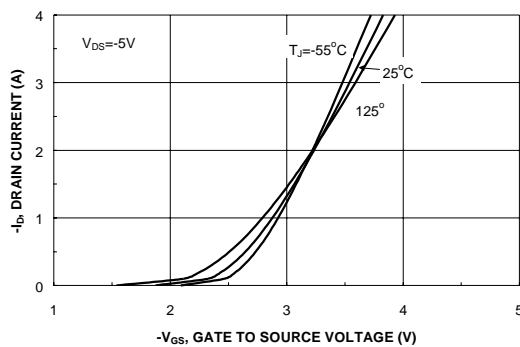


Figure 5. Transfer Characteristics.

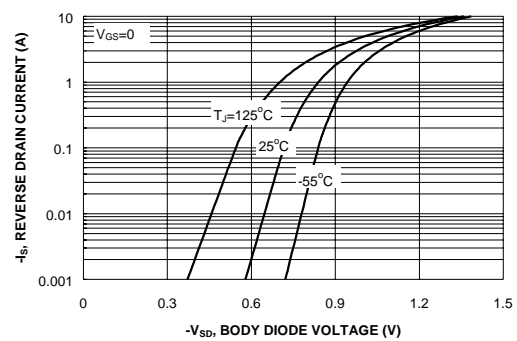


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

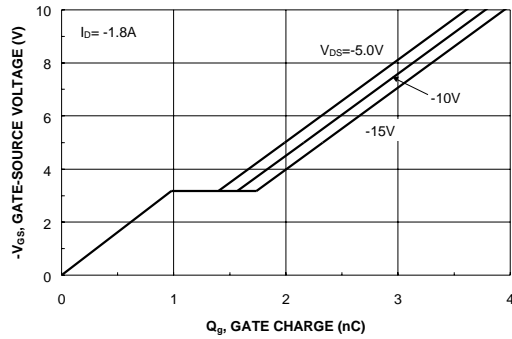


Figure 7. Gate-Charge Characteristics.

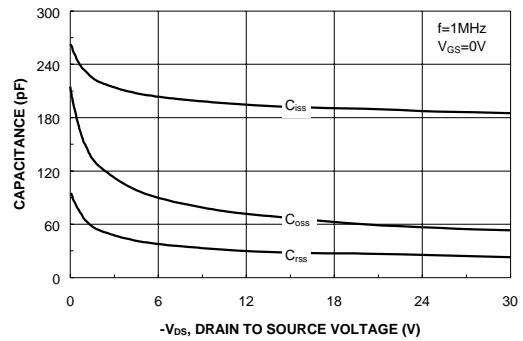


Figure 8. Capacitance Characteristics.

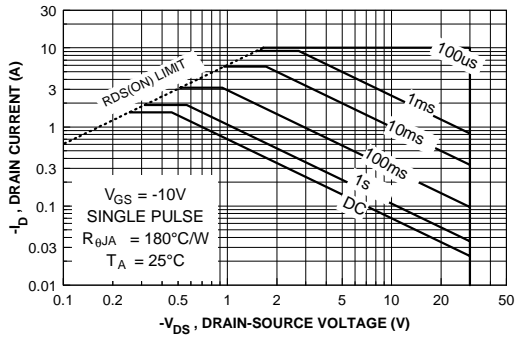


Figure 9. Maximum Safe Operating Area.

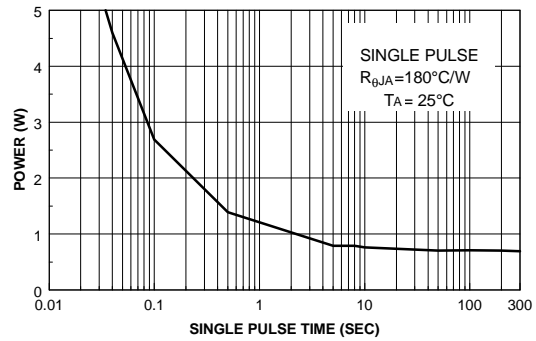


Figure 10. Single Pulse Maximum Power Dissipation.

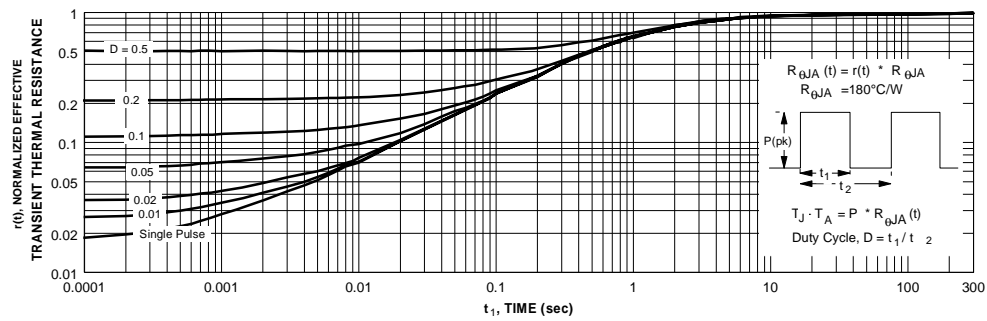


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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