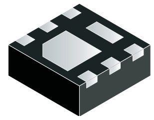


N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16301Q2

FEATURES

- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 2-mm × 2-mm Plastic Package

APPLICATIONS

- DC-DC Converters
- Battery and Load Management Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and load management applications. The SON 2x2 offers excellent thermal performance for the size of the package.

Top View

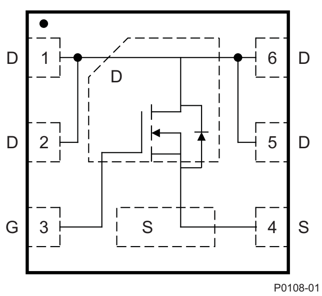


Table 1. PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (–4.5V)	2		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V	27	mΩ
		V_{GS} = 4.5V	23	mΩ
		V_{GS} = 8V	19	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

ORDERING INFORMATION

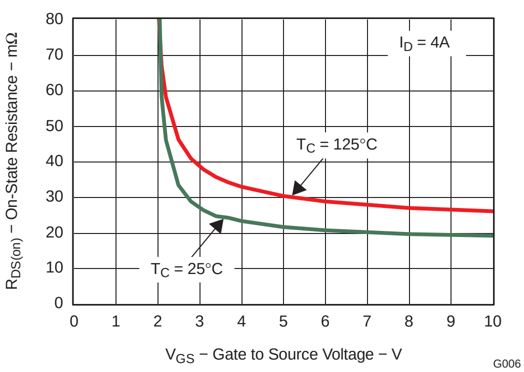
Device	Package	Media	Qty	Ship
CSD16301Q2	SON 2-mm × 2-mm Plastic Package	13-Inch Reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

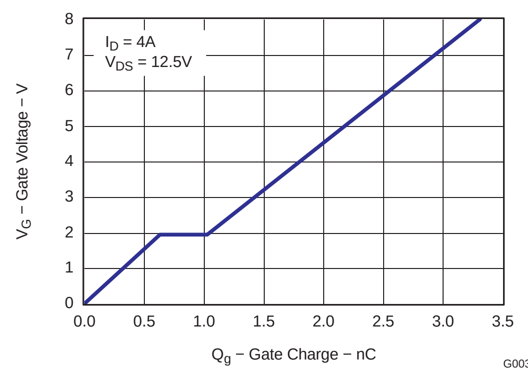
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	5	A
	Continuous Drain Current(1)	5	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	20	A
P_D	Power Dissipation(1)	2.3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 14A, L = 0.1mH, R_G = 25Ω	10	mJ

(1) Packaged Limited.
(2) Pulse duration 10μs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise specified

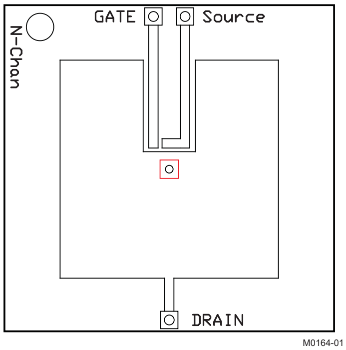
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250μA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/–8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250μA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V, I_{DS} = 4A		27	34	mΩ
		V_{GS} = 4.5V, I_{DS} = 4A		23	29	mΩ
		V_{GS} = 8V, I_{DS} = 4A		19	24	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 4A		16.5		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		260	340	pF
C_{OSS}	Output Capacitance			165	215	pF
C_{RSS}	Reverse Transfer Capacitance			13	17	pF
R_g	Series Gate Resistance			1.3	2.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 10V, I_{DS} = 4A		2	2.8	nC
Q_{gd}	Gate Charge – Gate to Drain			0.4		nC
Q_{gs}	Gate Charge Gate to Source			0.6		nC
Qg(th)	Gate Charge at Vth			0.3		nC
Q_{OSS}	Output Charge	V_{DS} = 12.5V, V_{GS} = 0V		3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_{DS} = 4A R_G = 2Ω		2.7		ns
t_r	Rise Time			4.4		ns
$t_{d(off)}$	Turn Off Delay Time			4.1		ns
t_f	Fall Time			1.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = 4A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 12.5V, I_F = 4A, di/dt = 200A/μs		5.1		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 12.5V, I_F = 4A, di/dt = 200A/μs		11		ns

THERMAL CHARACTERISTICS

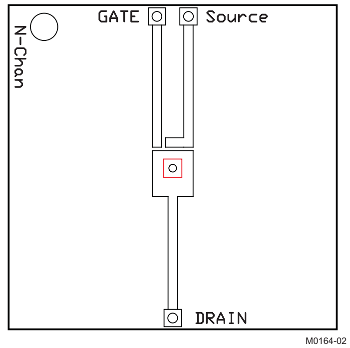
T_A = 25°C, unless otherwise specified

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (1)			8.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1) (2)			69	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 69°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 220°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

T_A = 25°C, unless otherwise specified

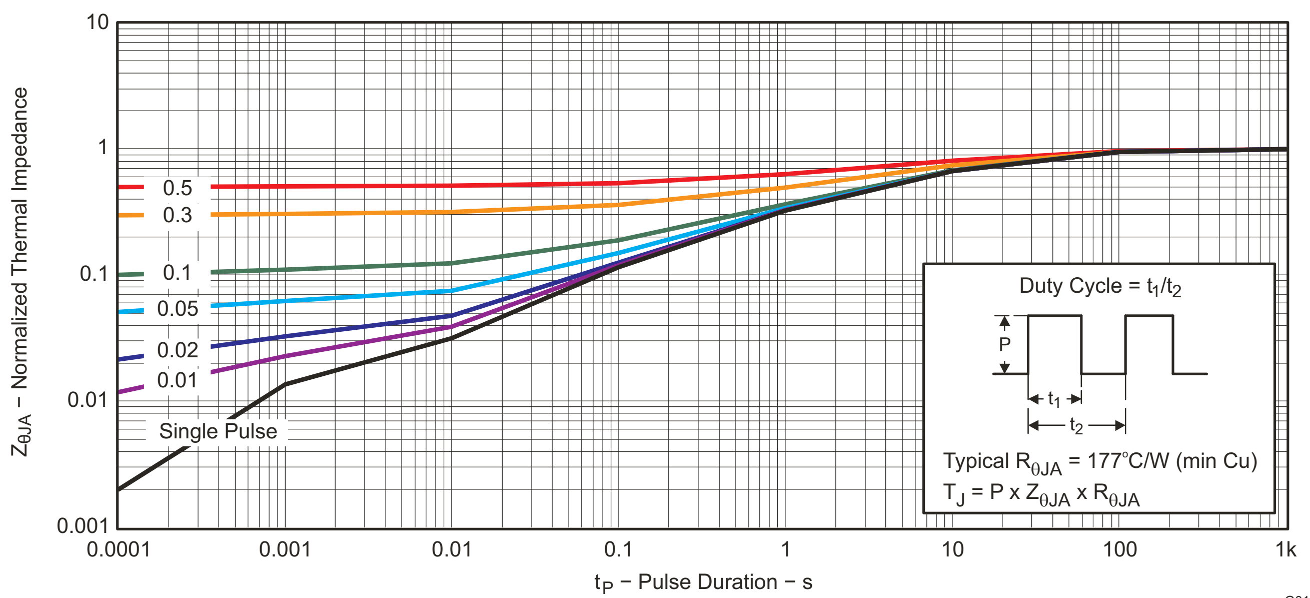


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise specified

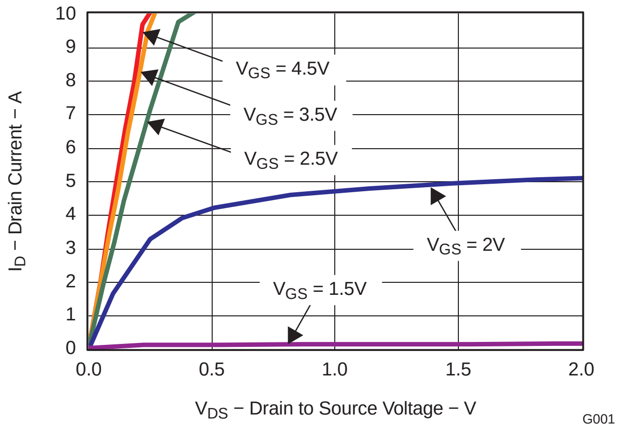


Figure 2. Saturation Characteristics

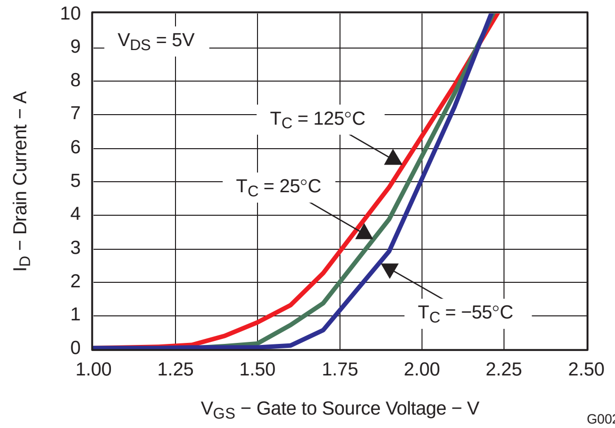


Figure 3. Transfer Characteristics

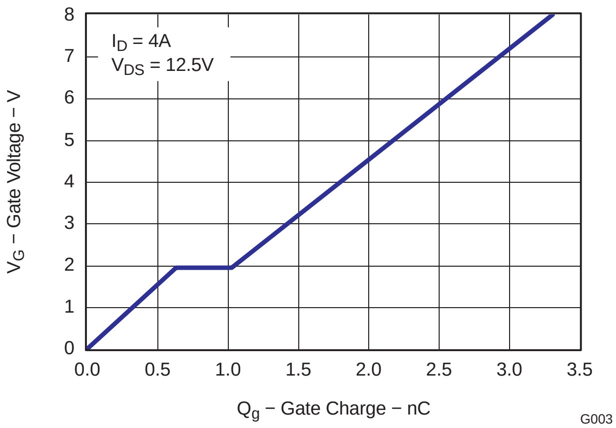


Figure 4. Gate Charge

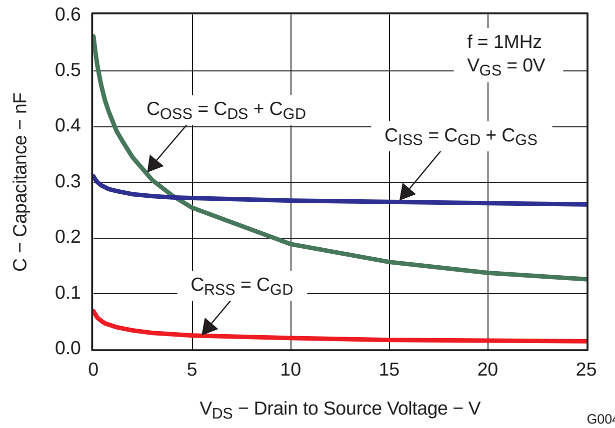


Figure 5. Capacitance

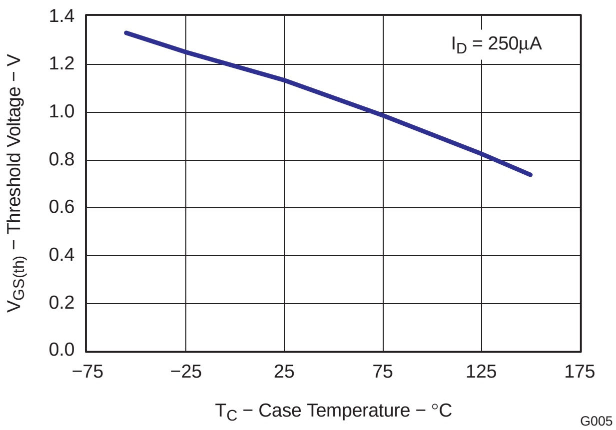


Figure 6. Threshold Voltage vs. Temperature

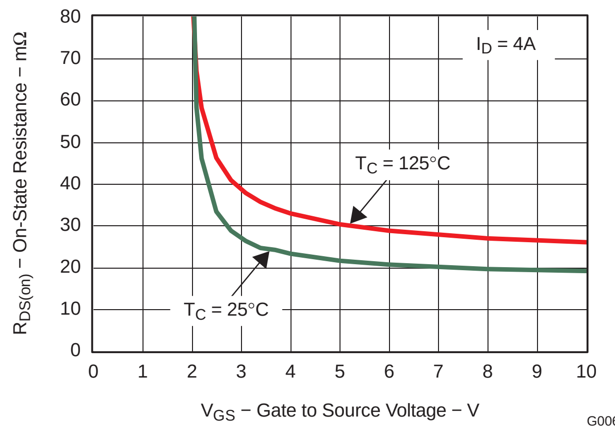


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise specified

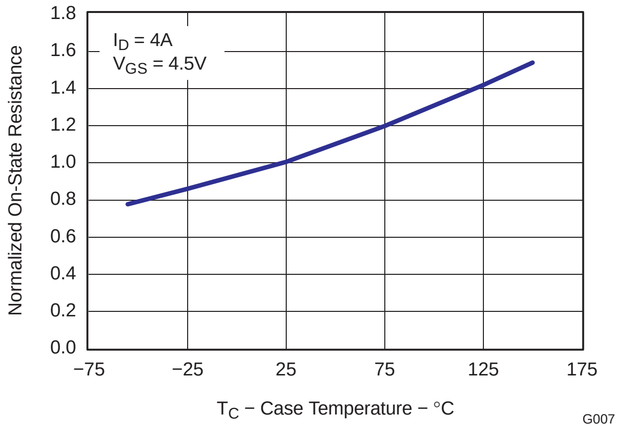


Figure 8. Normalized On-State Resistance vs. Temperature

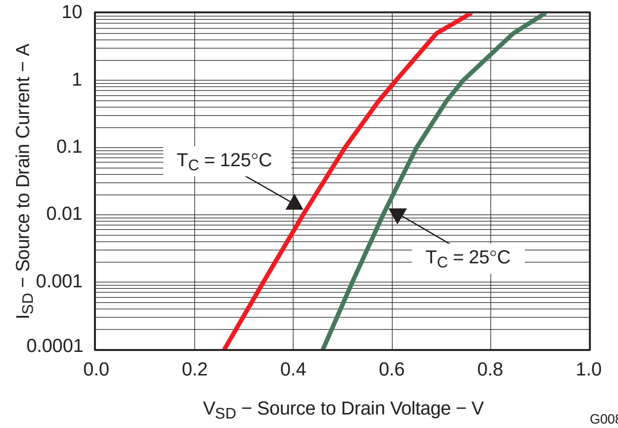


Figure 9. Typical Diode Forward Voltage

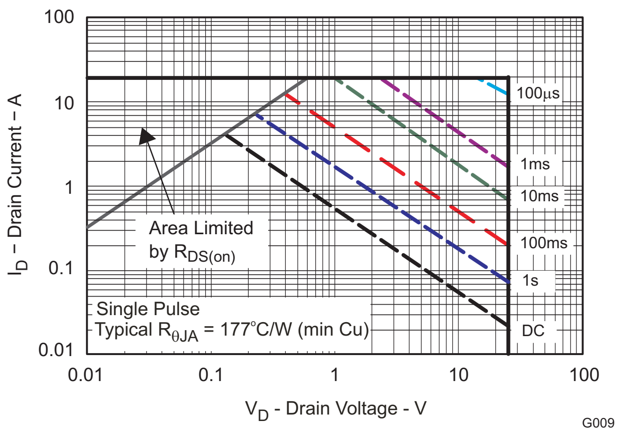


Figure 10. Maximum Safe Operating Area

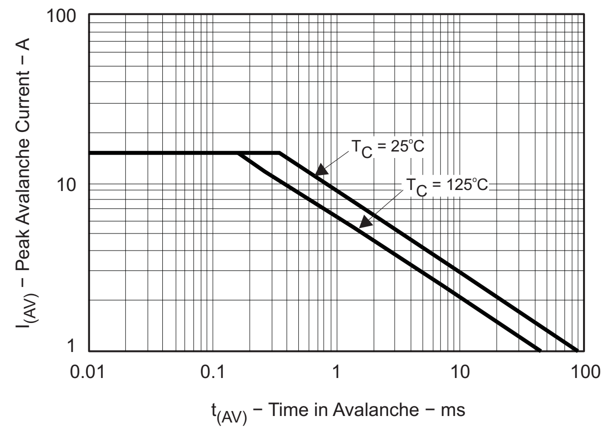


Figure 11.

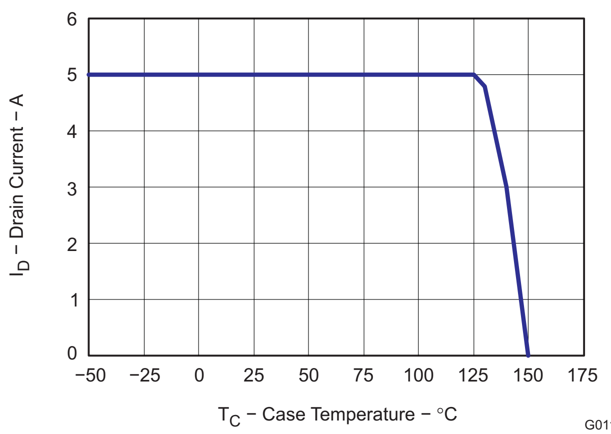
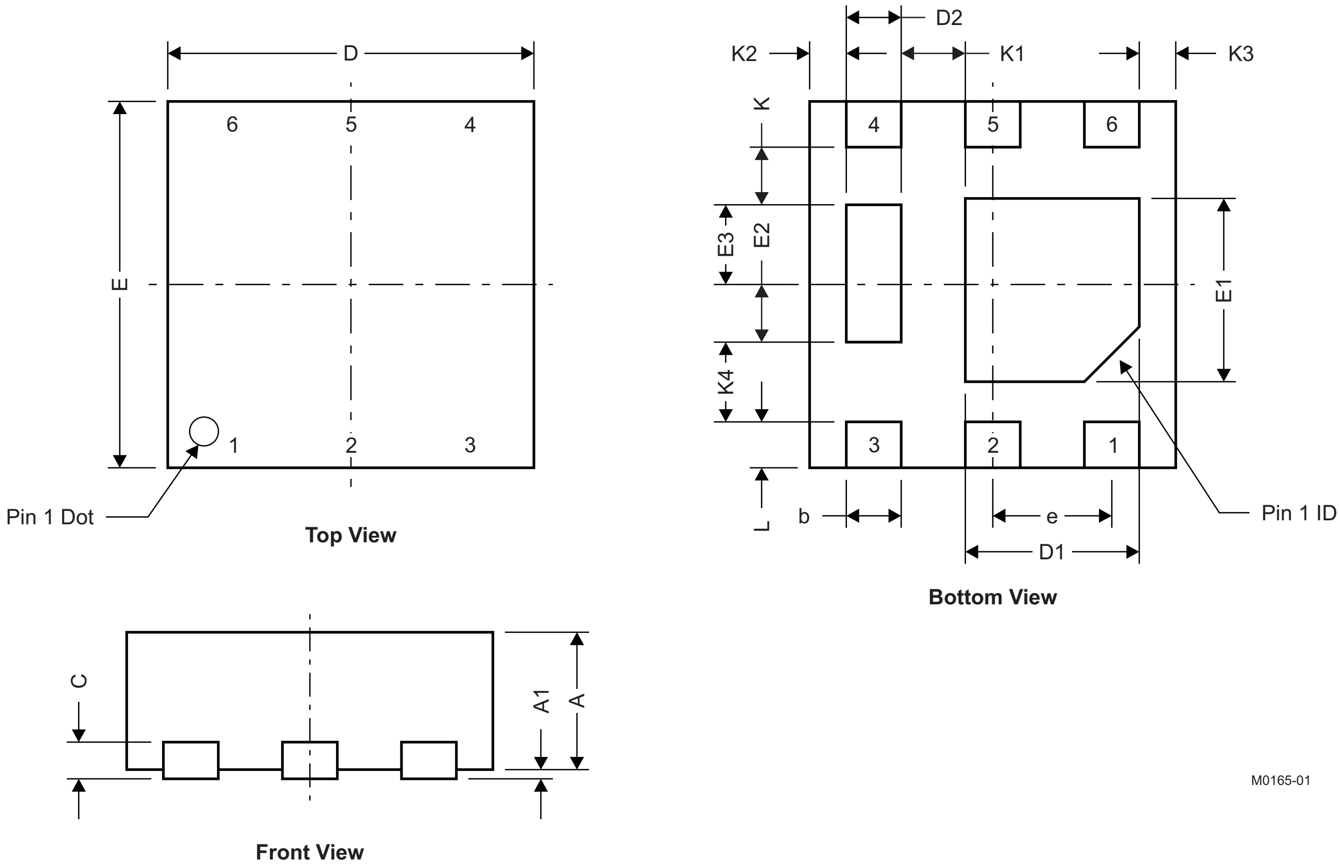


Figure 12. Maximum Drain Current vs. Temperature

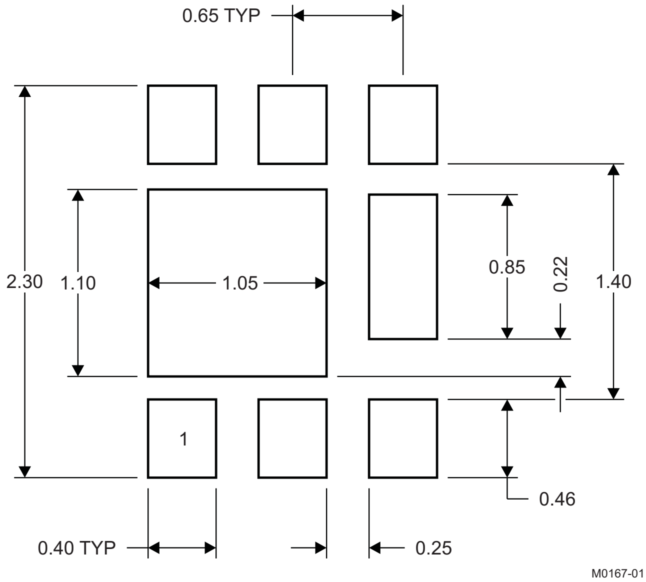
MECHANICAL DATA

Q2 Package Dimensions



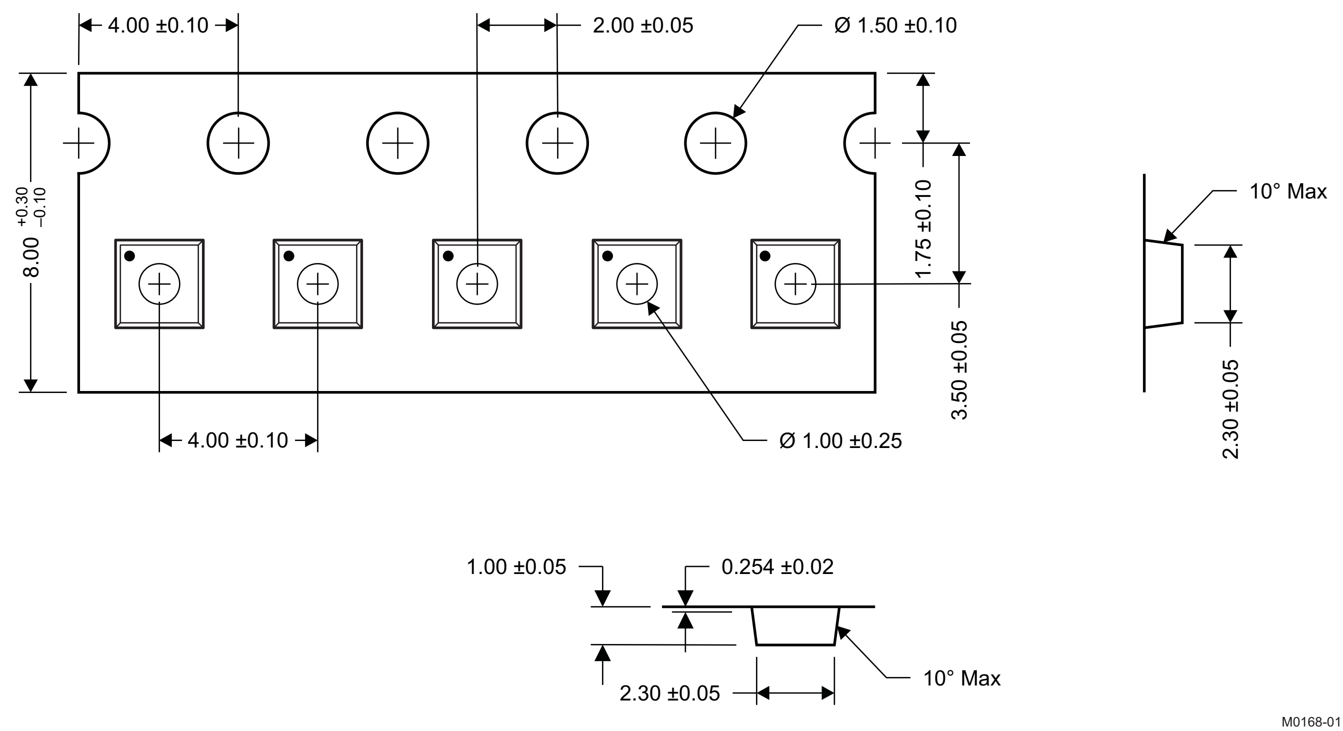
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q2 Tape and Reel Information



Notes:

1. Measured from centerline of spocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Measured from centerline of sprocket hole to centerline of pocket
4. Other material available
5. Typical SR of form tape Max 10^9 OHM/SQ
6. All dimensions are in mm, unless otherwise specified.

Package Marking Information

Location

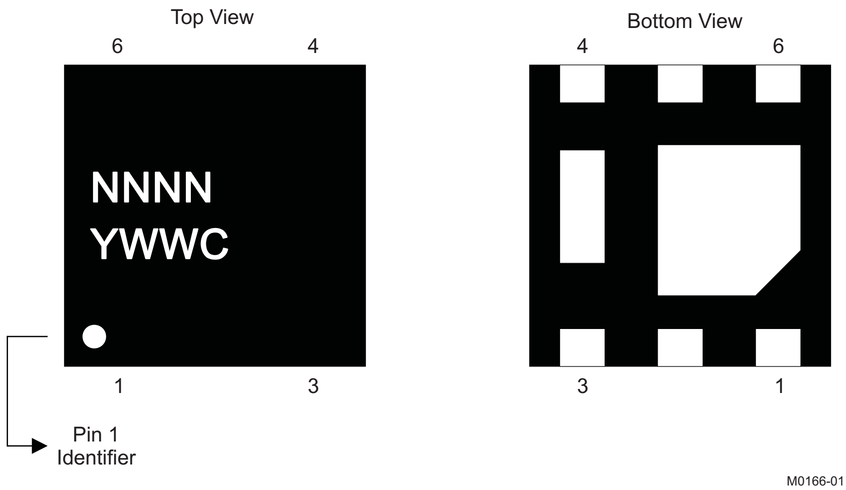
1st Line

NNNN = 4-digit Product Code

2nd Line (Date Code)

Y = Last digit of the Year
WW = 2-digit Work Week
C = Country of Origin
> Philippines = P
> Taiwan = T
> China = C
> Malaysia = M

Product Code = CSD16301
NNNN Mark = 1631



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CSD16301Q2	ACTIVE	SON	DQK	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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