ZWDK0001

PCI9054 FPGA development board technical information and data acquisition card circuit diagram source PCB project

- **OVERVIEW**

PCI development board is to meet FPGA users to learn and master this technology, and learn to use FPGA to achieve PCI interface communication and design development board, it contains a wealth of resources, it can be a variety of basic experiments and extended experiments on this platform. This manual is intended to users about major resource FPGA development board, develop routines and development methods, allowing users step by step to master FPGA system design.

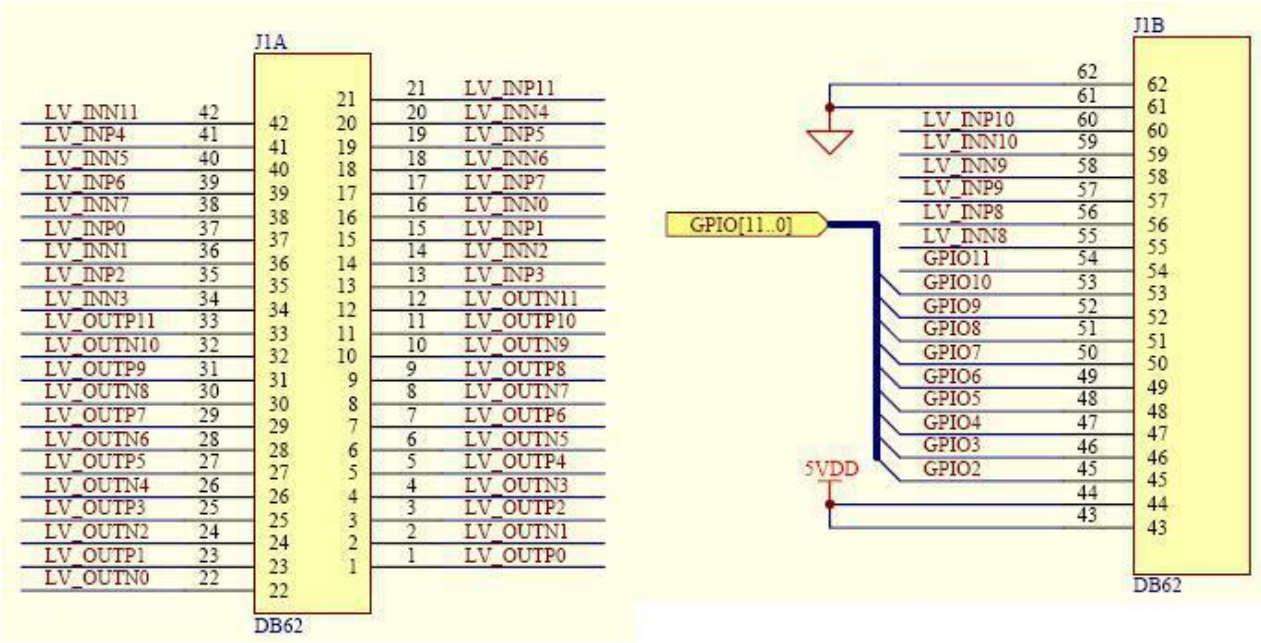
Hardware Resources
Development board includes the following resources:
(1) FPGA, type: EP1C12Q240;
(2) PCI, Model: PCI9054;
(3) LED, four;
(4) DIP switch, two;
(5) digital control, four were male;
(6) include the following interfaces:
a) 5V DC power supply;
b) LVDS output interface, 12 road;
c) LVDS input interface, 12 road;
d) GPIO interfaces, 47 road;
e) JTAG debug interface;
f) AS programming interface.

System power supply
The system supports two power supply: external DC 5V power supply, PCI power supply.

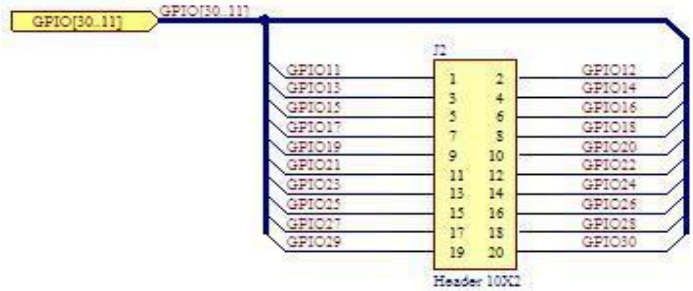
System Clock
(1) FPGA clock: 40MHz;
(2) User clock: Optional.

Test routine
(1) LED control experiment;
(2) Marquee experiment;
(3) Digital tube experiment;
(4) PCI reading test;
(5) PCI written test: PCI control LED, PCI control digital pipe;

External Interface



DB40 Interface: 37-way GPIO, 5V, 3.3V and ground.



SPECIFICATIONS

Photographed send mail. Are sent by mail, you can leave the mailbox photographed. Sell only data that does not contain PCB board.

This development board to sell all technical information, product-level design, materials include four-layer board PCB diagram, PC VC ++ source code,FPGA source code,PCI firmware, Protel circuit schematics and PCB plans, related documents and so on.

About:

High speed data acquisition board,It comes with: FPGA Verilog source code, Windows VC ++ source code and design documents

PCI interface circuit board with gold cheat

Interface: PCI9054C-PQFP176

FPGAChip:CYCLONE EP1C6Q240C8N

ConfigurationEEPROM:93LC66B

ExpandSDRAM:HY57V561620

FPGAConfiguration Program Chip:EPCS1

Clock Chip:50M

3.3VPower chip:tps78633

1.5VPower chip:LT1963-1.5

2.5VPower chip:LT1963-2.5

Power monitoring chip:MAX6306

- **The overall design strategy**

1.1Design strategy:

UsePLXThe company'sPCI9054ChipPCMachine andPCIData exchange between the cards, the use ofFPGAControlPCIInterfaces andLVDSData transfer between the interface, the use ofFPGAInternal storage resources to achieveFIFOData buffer between the two interfaces.

2.1 PCIInterface components:

PCIInterface Partially achievedPCICard andPCMachine data transfer.

The program usedPLXThe company9000Familypci9054ChipPCIConnection between bus and local bus,pci9054Is a use of morepciMaster chip, can becomepciMaster controller on the bus initiate data transfer, supportPCI 2.2Protocol specification, with two independentpciBetween bus and local busDMAChannel, SerialEEPROMInterfaces, as well as three local address space, and so on, the local bus operating clock frequency range0-50MHZ.

The program9054Working in modeCPlug and play andJTAGBoundary scan test, using finger inserted in the wayPCMachinePCISlot, use5V PCISlot Power,PCIEnd of work33MHZWorking frequency,32bitData width, the peak data transfer rate of132MB / SSustained transfer speed fromPCMachine hardware (memory, hard drives, motherboards) performance and software (operating systems, device drivers) performance jointly decided. The program, the use ofWindows 2000AndWindows XPOperating System (determined by the driver environment).

TypicalPCITiming in the following figure:

A transfer from thePCIMaster decided by a read or write operationC / BEDecision decoded address signal segment.

Twenty twoLocal interface section:

Partially achieved local interface9054VersusPCILocal bus data transfer card.

Pci9054Work of the local side haveinitiator,targetAndDMAThree ways. Among them,DMAWay is to use9054InsideDMAController to controlPCIEnd and the local end of the data transfer, in three ways in the most efficient, fastest, so this scheme usesDMAMode for data transmission. Pci9054The local operating clock frequency50MHZ, Sticky and logical useFPGATo achieve, byFPGAControlpci9054Timing local part of the work, the use of9054InsideDMAController to completeDMATransmission, data transmission isburstThe way. PC via software settings9054The register set9054After working mode and parameters, to submit data transfer tasks,PCIBus andlocalControl of the bus is9054InsideDMAThe controller takes over,DMAThe controller starts data transmission transfer, directly in the board storage space andPCRead and write operations between the machine's memory, the transmission process does not require PC software andPCMachineCPUParticipation, which greatly improves the efficiency and speed of data transmission.
TypicalDMAHow does the local bus read timing as shown below:

- **FPGALogical parts:**

FPGAThe logical part of the data buffer interface control and interface.
FPGAInternal logic is divided into three parts, namely:

- pci9054Local interface part, responsible forpci9054Timing control of the local interface.
- UseFPGAEmbeddedRAMBlock realizedFIFOBuffer section.
- LVDSInterface section, external interfaceLVDSLevel.

Twenty fourThe results
Using twoPCEach insert a machinePCICard approach to the way the test data to each otherPCICard performance transmission speed and transmission stability. The results show that, when the drive1-2Meters long25When the core cable, the card can transfer data at a steady rate(According to our own needs, inLVDSDrive within range), Under the correct operating conditions, there have been no error phenomenon test.9054The local bus load, the highest rate reached125MB / s.
Chip on the board are:
3.3VPower chip:tps78633
1.5VPower chip:LT1963-1.5
2.5VPower chip:LT1963-2.5
Power monitoring chip:MAX6306
PCIInterface chip:PLX9054
FPGAChip:CYCLONE EP1C6
ConfigurationEEPROM:93LC66B
ExpandSDRAM:HY57V561620
FPGAConfiguration Program Chip:EPCS1
50MClock Chip
Other parts of Five keys8Light-emitting diodes,JTAGAndASDownload the socket,FPGADebugging socket,3.3VPower indicator,1.5VPower indicator,2.5VPower indicator, parallel port25NeedleDB25Socket (for to-board transmissionLVDSSignal).