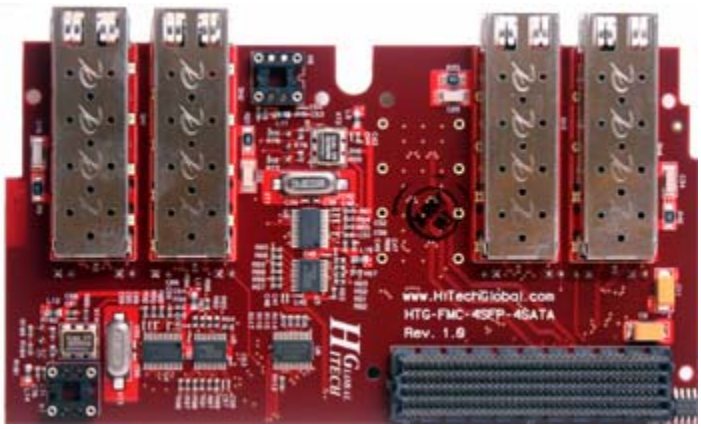
Vita57 Quad SFP/SATA FMC Module User Manual

HTG-FMC-X4SFP-X4SATA

Version 1.0 March 2010



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Revision History

Date	Version	Notes
3/12/2010	1.0	Preliminary

Table of Contents:

1) Introduction:

Vita 57 provides a mechanical standard for I/O mezzanine modules. This standard introduces a methodology that shall allow the front panel IO of IEEE 1101 form factor cards to be configured via mezzanine boards. Vita 57 modules have fixed locations for serial/parallel IOs, clocks, Jtag signals, VCC, and GND. HiTech Global's Vita 57 modules can be plugged into any Vita 57 based boards.

The FMC standard specifies Samtec's SEARAY™ connector set. The VITA 57 SEAM/SEAF Series system provides 400 I/Os in a 40 x 10 configuration or 160 I/Os in a selectively loaded 40 x 10 configuration, in 8.5mm and 10mm stack heights.

The Quad SFP/SATA FMC Module (HTG-FMC-X4SFP-X4SATA) is a FPGA Mezzanine Connector (FMC) daughter card with four SFP and FOUR Serial ATA (SATA) ports interfacing to total of 8 serial transceivers

2) Main Features:

- Four SFP Connectors
- Four SATA Connectors
- EEPROM
- FMC Connector
- Dedicated on-board Super Clock for each interface

3) Components Placement

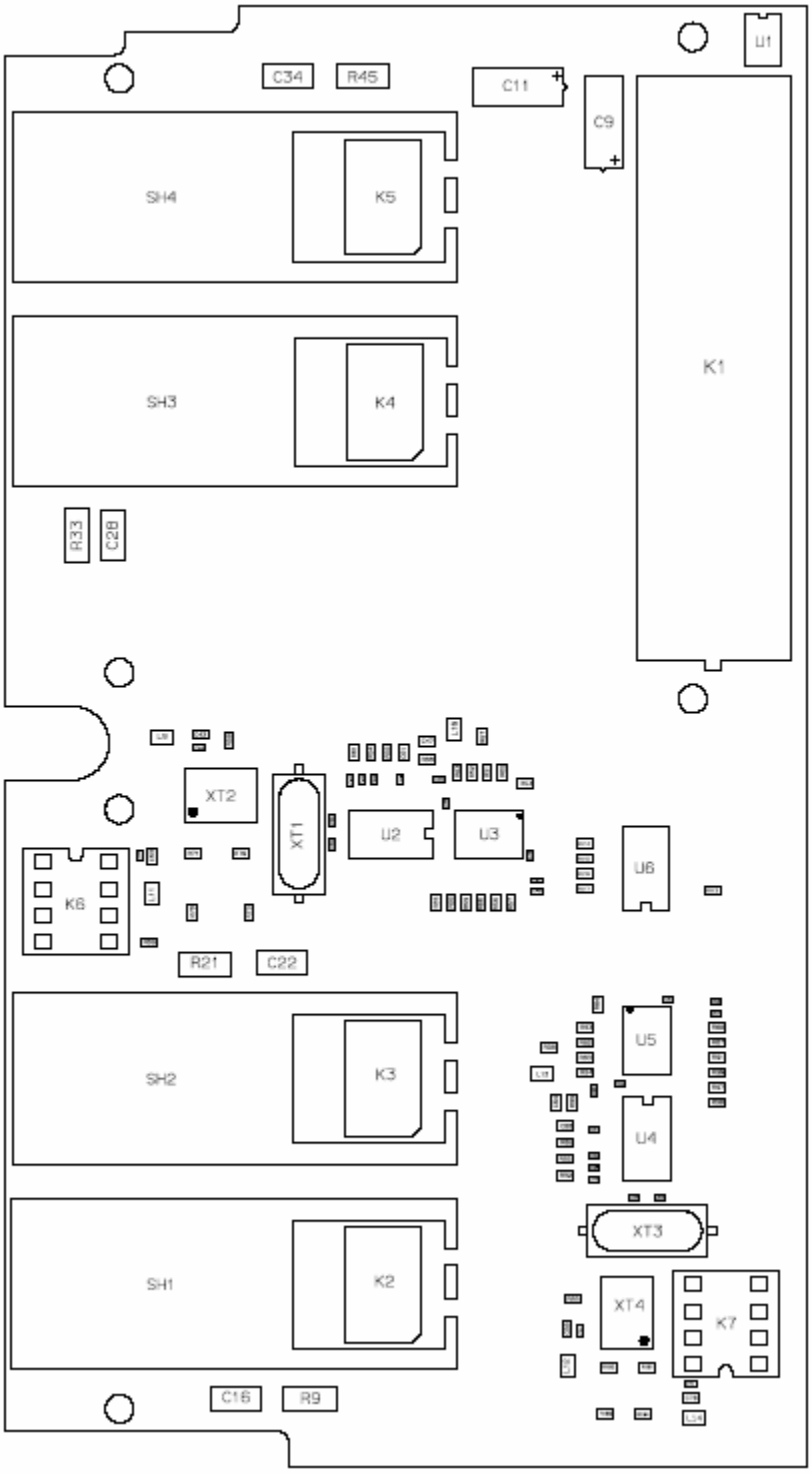


Figure (1): Primary Side

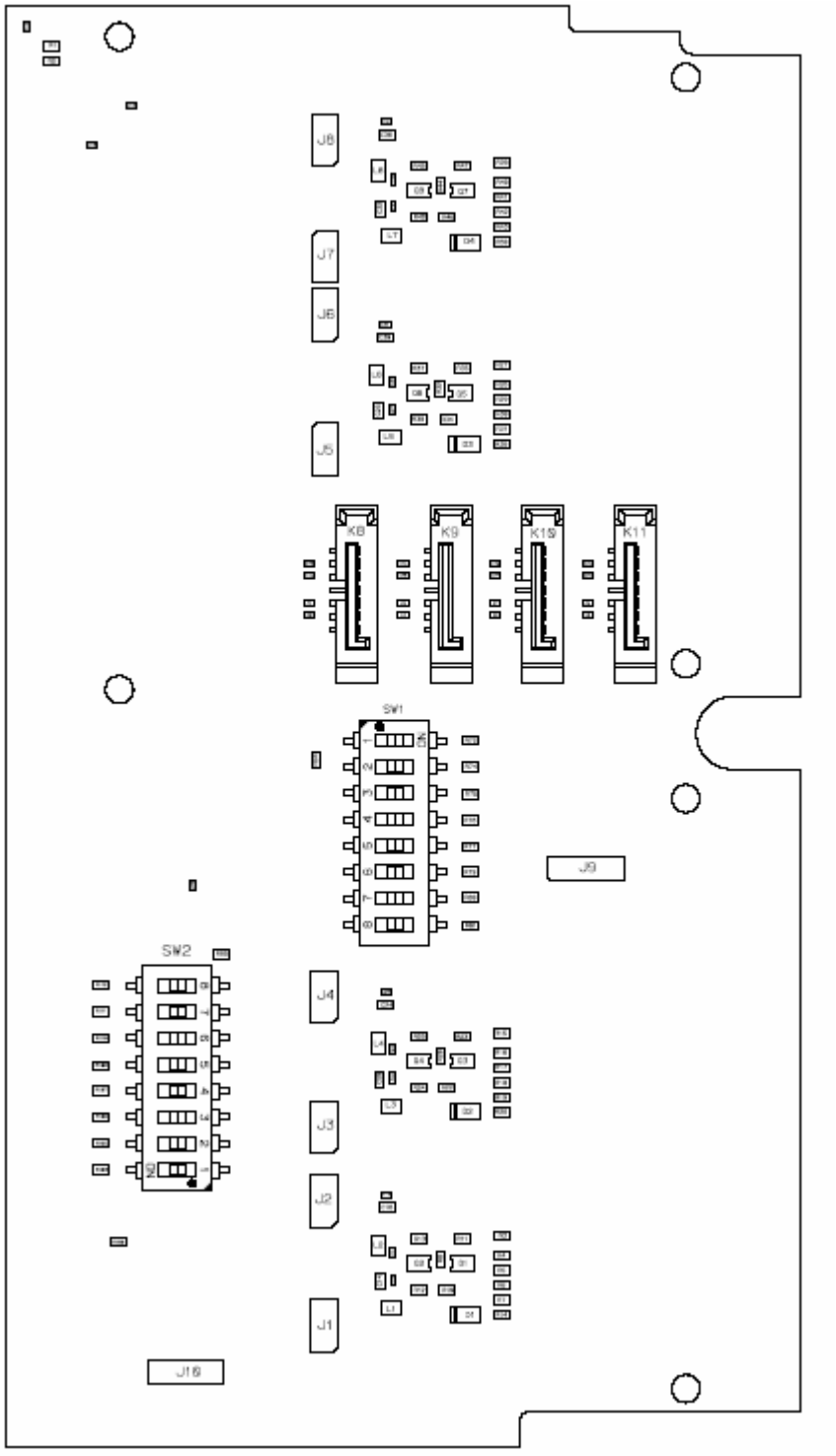


Figure (2): Secondary Side

4) SFP Interface

Four SFP cages are connected to four Serial transceivers through the FMC connector (DP4-DP7)

Tables (1-4) illustrate FMC pin assignment for the SFP ports.

SFP0 "K2" Pin Name	Signal Name	FMC Pin #	Note
SFP_LOS	LA01_CC_N	D9	
SFP_TX_ENABLE	LA00_CC_P	G6	J1: forced enable with no shunt, controlled by FMC with shunt
SFP_RATESEL	LA00_CC_N	G7	J2: forced full with no shunt, controlled by FMC with shunt
SFP_TX_FAULT	LA01_CC_P	D8	
SFP_DETECT	LA02_P	H7	
SFP_SDA	SDA_2	C31	Generated by I2C Multiplexer
SFP_SCL	SCL_2	C30	Generated by I2C Multiplexer
SFP _TXP	DP4_C2M_P	A34	
SFP_TXN	DP4_C2M_N	A35	
SFP_RXP	DP4_M2C_P	A14	
SFP_RXN	DP4_M2C_N	A15	

Table (1): FMC Pin Assignment for SFP0 "K2"

SFP1 "K3" Pin Name	Signal Name	FMC Pin #	Notes
SFP_LOS	LA04_P	H10	
SFP_TX_ENABLE	LA02_N	H8	J3: forced enable with no shunt, controlled by FMC with shunt
SFP_RATESEL	LA03_P	G9	J4: forced full with no shunt, controlled by FMC with shunt
SFP_TX_FAULT	LA03_N	G10	
SFP_DETECT	LA04_N	H11	
SFP_SDA	SDA_3	C31	Generated by I2C Multiplexer
SFP_SCL	SCL_3	C30	Generated by I2C Multiplexer
SFP _TXP	DP5_C2M_P	A38	
SFP_TXN	DP5_C2M_N	A39	
SFP_RXP	DP5_M2C_P	A18	
SFP_RXN	DP5_M2C_N	A19	

Table (2): FMC Pin Assignment for SFP1 "K3"

SFP2 "K4" Pin Name	Signal Name	FMC Pin #	Notes
SFP_LOS	LA06_N	C11	
SFP_TX_ENABLE	LA05_P	D11	J5: forced enable with no shunt, controlled by FMC with shunt
SFP_RATESEL	LA05_N	D12	J6: forced full with no shunt, controlled by FMC with shunt
SFP_TX_FAULT	LA06_P	C10	
SFP_DETECT	LA07_P	H13	
SFP_SDA	SDA_4	C31	Generated by I2C Multiplexer
SFP_SCL	SCL_4	C30	Generated by I2C Multiplexer
SFP _TXP	DP6_C2M_P	B36	
SFP_TXN	DP6_C2M_N	B37	
SFP_RXP	DP6_M2C_P	B16	
SFP_RXN	DP6_M2C_N	B13	

Table (3): FMC Pin Assignment for SFP2 "K4"

SFP3 "K5" Pin Name	Signal Name	FMC Pin #	Notes
SFP_LOS	LA09_P	D14	
SFP_TX_ENABLE	LA07_N	H14	J7: forced enable with no shunt, controlled by FMC with shunt
SFP_RATESEL	LA08_P	G12	J8: forced full with no shunt, controlled by FMC with shunt
SFP_TX_FAULT	LA08_N	G13	
SFP_DETECT	LA09_N	D15	
SFP_SDA	SDA_5	C31	Generated by I2C Multiplexer
SFP_SCL	SCL_5	C30	Generated by I2C Multiplexer
SFP _TXP	DP7_C2M_P	B32	
SFP_TXN	DP7_C2M_N	B33	
SFP_RXP	DP7_M2C_P	B12	
SFP_RXN	DP7_M2C_N	B13	

Table (4): FMC Pin Assignment for SFP3 "K5"

4.1) Clock Generation for SFP Connectors

Clock generation circuit for the SFP connectors uses the following components (all 4 ports share the same clock)

- Socket (K7) for user oscillator of choice – TEST_CLK
- Very low-jitter 25 MHz Silicon Lab **Si570 Oscillator** (XT4) – XTAL_IN1
- 25 MHz Crystal (XT3) – XTAL_IN0 and XTAL_OUT0
- **ICS843001-21** (U4) low phase noise LVPECL **Frequency Synthesizer**
- DIFFERENTIAL-TO-LVDS FANOUT BUFFER (U5)

The Si570 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. The Si570 is user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with <1 ppb resolution. The device is programmed via an I2C serial interface. Unlike traditional XO/VCXOs where a different crystal is required for each output frequency, the Si57x uses one fixed frequency crystal and a DSPLL clock synthesis IC to provide any-rate frequency operation. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability.

ICS843001-2 is a highly versatile, low phase noise LVPECL Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocksTM family of high performance clock solutions from IDT. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 26.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet.

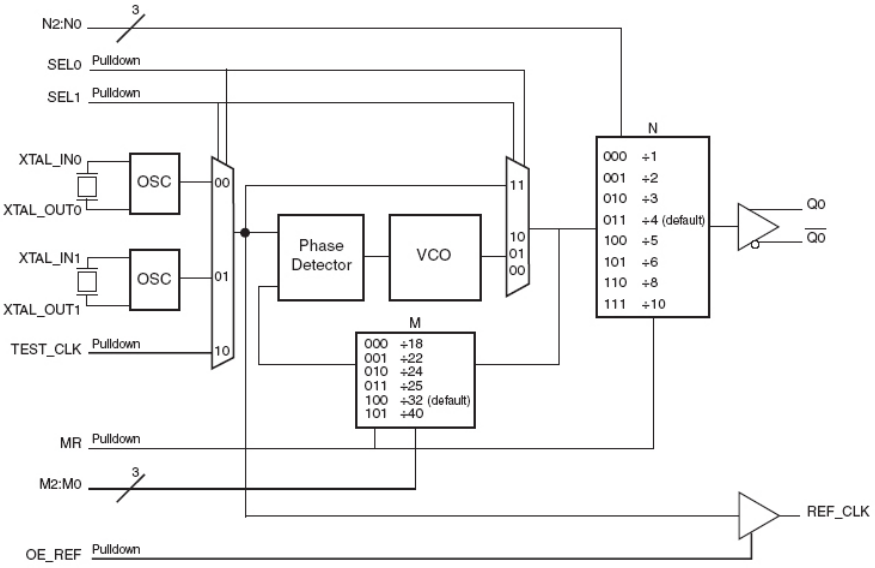


Figure (3): Frequency Synthesizer Block Diagram

Table (5) illustrates common configurations for different industry standard applications. Depending on value of the input frequency (through socket or on-board oscillators), "M", and "N" divider values users can generate different output frequencies.

*** Example for generating 125 MHz by using a 25 MHz oscillator:

Output frequency = (25MHz) *(25) / 5 = 625/5 = 125 MHz

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
24.75	24	8	594	74.25	HDTV
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
25	**25**	**4**	**625**	**156.25**	**10 GigE**
25	**25**	**5**	**625**	**125**	**1 GigE**
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	5	562.5	187.5	12 GigE

Table (5) Frequency Synthesizer Common Configuration Table

Table (6), (7), and (8) illustrate selection of "M", "N", and "Clock Source". Table (9) illustrates SW2 Dip Switch setting based on selected values of the above mentioned parameters.

Inputs				Input Frequency (MHz)	
M2	M1	M0	M Divider Value	Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

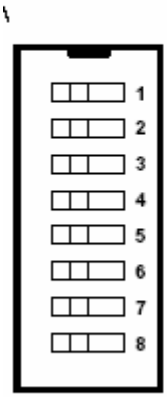
Table (6) Frequency Synthesizer Programmable "M" Output Divider Function Table

Inputs			
N2	N1	N0	M Divider Value
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table (7) Frequency Synthesizer Programmable "N" Output Divider Function Table

Inputs			
SEL1	SEL0	Reference	PLL Mode
0	0	XTAL0	1
0	1	XTAL1	2
1	0	TEST_CLK	8
1	1	TEST_CLK1	10

Table (8) Frequency Synthesizer Bypass Mode Function Table



DipSwitch Number	ICS Conf.Pin Name	Logic State	
		DipSw. ON	DipSw. OFF
1	N0	0	1
2	N1	0	1
3	N2	0	1
4	M0	0	1
5	M1	0	1
6	M2	0	1
7	SEL0	0	1
8	SEL1	0	1

Table (9) Frequency Synthesizer SW2 DIP Switch Setting

5) SATA Interface

Four SATA ports are connected to four Serial transceivers through the FMC connectors (DP0-DP3)

Tables (10-13) illustrate FMC pin assignment for the SATA ports.

SATA0 "K8" Pin Name	Signal Name	FMC Pin #	Note
SATA0 _TXP	DP0_C2M_P	C2	
SATA0 _TXN	DP0_C2M_N	C3	
SATA0 _RXP	DP0_M2C_P	C6	
SATA0 _RXN	DP0_M2C_N	C7	

Table (10): FMC Pin Assignment for SATA "K8"

SATA1 "K9" Pin Name	Signal Name	FMC Pin #	Note
SATA1 _TXP	DP1_C2M_P	A22	
SATA1 _TXN	DP1_C2M_N	A23	
SATA1 _RXP	DP1_M2C_P	A2	
SATA1 _RXN	DP1_M2C_N	A3	

Table (11): FMC Pin Assignment for SATA "K9"

SATA2 "K10" Pin Name	Signal Name	FMC Pin #	Note
SATA2 _TXP	DP2_C2M_P	A26	
SATA2 _TXN	DP2_C2M_N	A27	
SATA2 _RXP	DP2_M2C_P	A6	
SATA2 _RXN	DP2_M2C_N	A7	

Table (12): FMC Pin Assignment for SATA "K10"

SATA3 "K11" Pin Name	Signal Name	FMC Pin #	Note
SATA3 _TXP	DP3_C2M_P	A30	
SATA3 _TXN	DP3_C2M_N	A31	
SATA3 _RXP	DP3_M2C_P	A10	
SATA3 _RXN	DP3_M2C_N	A11	

Table (13): FMC Pin Assignment for SATA "K11"

5.1) Clock Generation for SATA Connectors

Clock generation circuit for the SATA connectors uses the following components (all 4 ports share the same clock)

- Socket (K6) for user oscillator of choice – TEST_CLK
- Very low-jitter 25 MHz Silicon Lab **Si570 Oscillator** (XT2) – XTAL_IN1
- 25 MHz Crystal (XT1) – XTAL_IN0 and XTAL_OUT0
- **ICS843001-21** (U2) low phase noise LVPECL **Frequency Synthesizer**
- DIFFERENTIAL-TO-LVDS FANOUT BUFFER (U3)

The Si570 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at any frequency. The Si570 is user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with <1 ppb resolution. The device is programmed via an I2C serial interface. Unlike traditional XO/VCXOs where a different crystal is required for each output frequency, the Si57x uses one fixed frequency crystal and a DSPLL clock synthesis IC to provide any-rate frequency operation. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability.

ICS843001-2 is a highly versatile, low phase noise LVPECL Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocksTM family of high performance clock solutions from IDT. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e.

1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 26.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet.

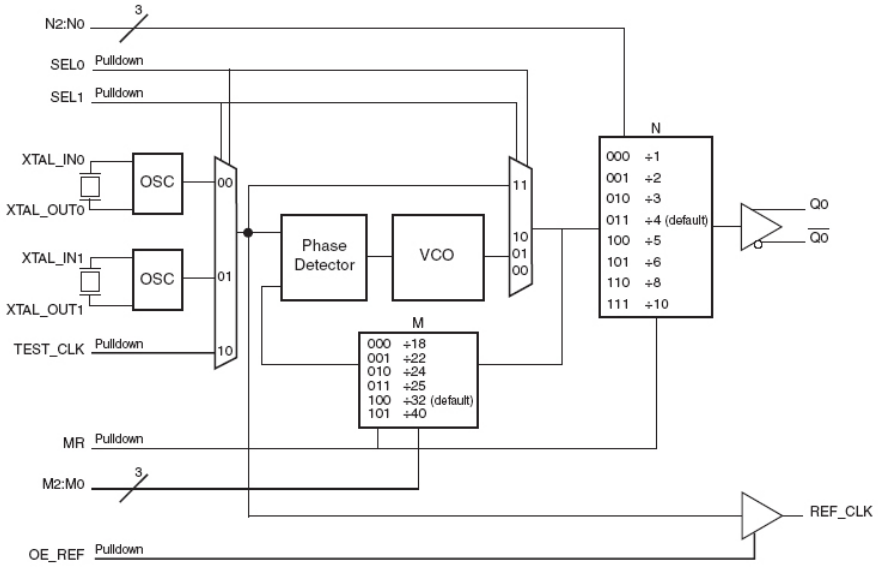


Figure (4): Frequency Synthesizer Block Diagram

Table (14) illustrates common configurations for different industry standard applications. Depending on value of the input frequency (through socket or on-board oscillators), "M", and "N" divider values users can generate different output frequencies.

*** Example for generating 150 MHz by using a 25 MHz oscillator:
Output frequency = (25MHz) *(24) / 4 = 600/4 = 150 MHz

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
24.75	24	8	594	74.25	HDTV
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
25	25	4	625	156.25	10 GigE
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	**24**	**4**	**600**	**150**	**SATA**
25	**24**	**8**	**600**	**75**	**SATA**
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	5	562.5	187.5	12 GigE

Table (14) Frequency Synthesizer Common Configuration Table

Table (15), (16), and (17) illustrate selection of "M", "N", and "Clock Source". Table (18) illustrates SW1 Dip Switch setting based on selected values of the above mentioned parameters.

Inputs				Input Frequency (MHz)	
M2	M1	M0	M Divider Value	Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

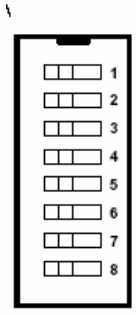
Table (15) Frequency Synthesizer Programmable "M" Output Divider Function Table

Inputs			
N2	N1	N0	M Divider Value
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table (16) Frequency Synthesizer Programmable "N" Output Divider Function Table

Inputs			
SEL1	SEL0	Reference	PLL Mode
0	0	XTAL0	1
0	1	XTAL1	2
1	0	TEST_CLK	8
1	1	TEST_CLK1	10

Table (17) Frequency Synthesizer Bypass Mode Function Table



DipSwitch Number	ICS Conf.Pin Name	Logic State	
		DipSw. ON	DipSw. OFF
1	N0	0	1
2	N1	0	1
3	N2	0	1
4	M0	0	1
5	M1	0	1
6	M2	0	1
7	SEL0	0	1
8	SEL1	0	1

Table (18) Frequency Synthesizer SW1 DIP Switch Setting

6) FMC Interface

The SFP+ Module is populated with a 400-pin Samtec connector for implementation of Vita 57 FPGA Mezzanine Card (FMC) interface. The Vita57 calls for fixed location of IOs, Power, Clocks, and JTAG signals so any compliant module can easily be pluggable into any compliant carrier card.

The FMC connector provides access to 8 Serial Transceivers (on the FPGA side) JTAG signals, 12V/3.3V/Adjustable supplies, I2C signals, and multiple differential clocks.

Table (19) and (20) illustrate the pin assignment for the FMC connector interface.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table (19): FMC Pin Assignment

	Column "B"				Column "A"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	RES1	Reserved		1	GND	-	
2	GND	-		2	DP1_M2C_P	SATA1 RXDATA_P	
3	GND	-		3	DP1_M2C_N	SATA1 RXDATA_N	
4	DP9_M2C_P	NC		4	GND	-	
5	DP9_M2C_N	NC		5	GND	-	
6	GND	-		6	DP2_M2C_P	SATA2 RXDATA_P	
7	GND	-		7	DP2_M2C_N	SATA2 RXDATA_N	
8	DP8_M2C_P	NC		8	GND	-	
9	DP8_M2C_N	NC		9	GND	-	
10	GND	-		10	DP3_M2C_P	SATA3 RXDATA_P	
11	GND	-		11	DP3_M2C_N	SATA3 RXDATA_N	
12	DP7_M2C_P	SFP3 RXDATA_P		12	GND	-	
13	DP7_M2C_N	SFP3 RXDATA_N		13	GND	-	
14	GND	-		14	DP4_M2C_P	SFP0 RXDATA_P	
15	GND	-		15	DP4_M2C_N	SFP0 RXDATA_N	
16	DP6_M2C_P	SFP2 RXDATA_P		16	GND	-	
17	DP6_M2C_N	SFP2 RXDATA_N		17	GND	-	
18	GND	-		18	DP5_M2C_P	SFP1 RXDATA_P	
18	GND	-		18	DP5_M2C_N	SFP1 RXDATA_N	
20	GBTCLK1_M2C_P	SFP_REF_CLK1_P		20	GND	-	
21	GBTCLK1_M2C_N	SFP_REF_CLK1_P		21	GND	-	
22	GND	-		22	DP1_C2M_P	SATA1TXDATA_P	
23	GND	-		23	DP1_C2M_N	SATA1 TXDATA_N	
24	DP9_C2M_P	NC	NC	24	GND	-	
25	DP9_C2M_N	NC	NC	25	GND	-	
26	GND	-		26	DP2_C2M_P	SATA2 TXDATA_P	
27	GND	-		27	DP2_C2M_N	SATA2 TXDATA_N	
28	DP8_C2M_P	NC	NC	28	GND	-	
29	DP8_C2M_N	NC	NC	29	GND	-	
30	GND	-		30	DP3_C2M_P	SATA3 TXDATA_P	
31	GND	-		31	DP3_C2M_N	SATA3 TXDATA_N	
32	DP7_C2M_P	SFP3 TXDATA_P		32	GND	-	
33	DP7_C2M_N	SFP3 TXDATA_N		33	GND	-	
34	GND	-		34	DP4_C2M_P	SFP0 TXDATA_P	
35	GND	-		35	DP4_C2M_N	SFP0 TXDATA_N	
36	DP6_C2M_P	SFP2 TXDATA_P		36	GND	-	
37	DP6_C2M_N	SFP2 TXDATA_N		37	GND	-	
38	GND	-		38	DP5_C2M_P	SFP1 TXDATA_P	
39	GND	-		39	DP5_C2M_N	SFP1TXDATA_N	
40	RES0	NC		40	GND	-	

	Column "D"				Column " C"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	PG_C2M	Power Good		1	GND	NC	
2	GND			2	DP0_C2M_P	SATA0 TXDATA_P	
3	GND			3	DP0_C2M_N	SATA0 TXDATA_N	
4	GBTCLK0_M2C_P	SATA_REF_CLK_P		4	GND		
5	GBTCLK0_M2C_N	SATA_REF_CLK_P		5	GND		
6	GND			6	DP0_M2C_P	SATA0 RXDATA_P	
7	GND			7	DP0_M2C_N	SATA0 RXDATA_N	
8	LA01_P_CC	User defined signal	NC	8	GND		
9	LA01_N_CC	User defined signal	NC	9	GND		
10	GND			10	LA06_P		NC
11	LA05_P	User defined signal	NC	11	LA06_N		NC
12	LA05_N	User defined signal	NC	12	GND		
13	GND			13	GND		
14	LA09_P	User defined signal	NC	14	LA10_P		NC
15	LA09_N	User defined signal	NC	15	LA10_N		NC
16	GND			16	GND		
17	LA13_P	User defined signal	NC	17	GND		
18	LA13_N	User defined signal	NC	18	LA14_P		NC
18	GND			18	LA14_N		NC
20	LA17_P_CC	User defined signal	NC	20	GND		
21	LA17_N_CC	User defined signal	NC	21	GND		
22	GND			22	LA18_P_CC		NC
23	LA23_P	User defined signal	NC	23	LA18_N_CC		NC
24	LA23_N	User defined signal	NC	24	GND		
25	GND			25	GND		
26	LA26_P	User defined signal	NC	26	LA27_P		NC
27	LA26_N	User defined signal	NC	27	LA27_N		NC
28	GND			28	GND		
29	TCK	JTAG		29	GND		
30	TDI	JTAG BYPASS		30	SCL	I2C serial clock.	
31	TDO	JTAG		31	SDA	I2C serial data.	
32	3P3VAUX	3.3V Aux. Supply	3.3V	32	GND	-	-
33	TMS	JTAG		33	GND	-	-
34	TRST_L	Asynch. Init.		34	GA0	Geographical address	
35	GA1	Geographical address	U5-2	35	12P0V	12V Supply	
36	3P3V	3.3V Supply	3.3V	36	GND		
37	GND		GND	37	12P0V	12V Supply	
38	3P3V	3.3V Supply	3.3V	38	GND		
39	GND		GND	39	3P3V	3.3V Supply	
40	3P3V	3.3V Supply	3.3V	40	GND		

	Column "F"				Column "E"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	PG_M2C	Power Good		1	GND	GND	GND
2	GND	GND	GND	2	HA01_P_CC	User defined signal	NC
3	GND	GND	GND	3	HA01_N_CC	User defined signal	NC
4	HA00_P_CC	User defined signal	NC	4	GND	GND	GND
5	HA00_N_CC	User defined signal	NC	5	GND	GND	GND
6	GND	GND	GND	6	HA05_P	User defined signal	NC
7	HA04_P	User defined signal	NC	7	HA05_N	User defined signal	NC
8	HA04_N	User defined signal	NC	8	GND	GND	GND
9	GND	GND	GND	9	HA09_P	User defined signal	NC
10	HA08_P	User defined signal	NC	10	HA09_N	User defined signal	NC
11	HA08_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	HA13_P	User defined signal	NC
13	HA12_P	User defined signal	NC	13	HA13_N	User defined signal	NC
14	HA12_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	HA16_P	User defined signal	NC
16	HA15_P	User defined signal	NC	16	HA16_N	User defined signal	NC
17	HA15_N	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	HA20_P	User defined signal	NC
18	HA19_P	User defined signal	NC	18	HA20_N	User defined signal	NC
20	HA19_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	HB03_P	User defined signal	NC
22	HB02_P	User defined signal	NC	22	HB03_N	User defined signal	NC
23	HB02_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	HB05_P	User defined signal	NC
25	HB04_P	User defined signal	NC	25	HB05_N	User defined signal	NC
26	HB04_N	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	HB09_P	User defined signal	NC
28	HB08_P	User defined signal	NC	28	HB09_N	User defined signal	NC
29	HB08_N	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	HB13_P	User defined signal	NC
31	HB12_P	User defined signal	NC	31	HB13_N	User defined signal	NC
32	HB12_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	HB19_P	User defined signal	NC
34	HB16_P	User defined signal	NC	34	HB19_N	User defined signal	NC
35	HB16_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	HB21_P	User defined signal	NC
37	HB20_P	User defined signal	NC	37	HB21_N	User defined signal	NC
38	HB20_N	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VADJ	Adjustable Voltage	
40	VADJ	Adjustable Voltage		40	GND	GND	GND

	Column "H"				Column "G"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	VREF_A_M2C	Reference voltage		1	GND	GND	GND
2	PRSNT_M2C_L	Present Signal		2	CLK1_M2C_P	Differential Clock	NC
3	GND	GND	GND	3	CLK1_M2C_N	Differential Clock	NC
4	CLK0_M2C_P	Differential Clock	NC	4	GND	GND	GND
5	CLK0_M2C_N	Differential Clock	NC	5	GND	GND	GND
6	GND	GND	GND	6	LA00_P_CC	User defined signal	NC
7	LA02_P	User defined signal	NC	7	LA00_N_CC	User defined signal	NC
8	LA02_N	User defined signal	NC	8	GND	GND	GND
9	GND	GND	GND	9	LA03_P	User defined signal	NC
10	LA04_P	User defined signal	NC	10	LA03_N	User defined signal	NC
11	LA04_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	LA08_P	User defined signal	NC
13	LA07_P	User defined signal	NC	13	LA08_N	User defined signal	NC
14	LA07_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	LA12_P	User defined signal	NC
16	LA11_P	User defined signal	NC	16	LA12_N	User defined signal	NC
17	LA11_N	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	LA16_P	User defined signal	NC
18	LA15_P	User defined signal	NC	18	LA16_N	User defined signal	NC
20	LA15_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	LA20_P	User defined signal	NC
22	LA19_P	User defined signal	NC	22	LA20_N	User defined signal	NC
23	LA19_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	LA22_P	User defined signal	NC
25	LA21_P	User defined signal	NC	25	LA22_N	User defined signal	NC
26	LA21_N	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	LA25_P	User defined signal	NC
28	LA24_P	User defined signal	NC	28	LA25_N	User defined signal	NC
29	LA24_N	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	LA29_P	User defined signal	NC
31	LA28_P	User defined signal	NC	31	LA29_N	User defined signal	NC
32	LA28_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	LA31_P	User defined signal	NC
34	LA30_P	User defined signal	NC	34	LA31_N	User defined signal	NC
35	LA30_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	LA33_P	User defined signal	NC
37	LA32_P	User defined signal	NC	37	LA33_N	User defined signal	NC
38	LA32_N	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VADJ	Adjustable Voltage	
40	VADJ	Adjustable Voltage		40	GND		

	Column "K"				Column "J"		
	FMC Pin Name	Pin Description	DEST.		FMC Pin Name	Pin Description	DEST.
1	VREF_B_M2C	Reference voltage		1	GND	GND	GND
2	GND	GND	GND	2	CLK3_M2C_P	Differential Clock	NC
3	GND	GND	GND	3	CLK3_M2C_N	Differential Clock	NC
4	CLK2_M2C_P	Differential Clock	NC	4	GND	GND	GND
5	CLK2_M2C_N	Differential Clock	NC	5	GND	GND	GND
6	GND	GND	GND	6	HA03_P	User defined signal	NC
7	HA02_P	User defined signal	NC	7	HA03_N	User defined signal	NC
8	HA02_N	User defined signal	NC	8	GND	GND	GND
9	GND	GND	GND	9	HA07_P	User defined signal	NC
10	HA06_P	User defined signal	NC	10	HA07_N	User defined signal	NC
11	HA06_N	User defined signal	NC	11	GND	GND	GND
12	GND	GND	GND	12	HA11_P	User defined signal	NC
13	HA10_P	User defined signal	NC	13	HA11_N	User defined signal	NC
14	HA10_N	User defined signal	NC	14	GND	GND	GND
15	GND	GND	GND	15	HA14_P	User defined signal	NC
16	HA17_P_CC	User defined signal	NC	16	HA14_N	User defined signal	NC
17	HA17_N_CC	User defined signal	NC	17	GND	GND	GND
18	GND	GND	GND	18	HA18_P	User defined signal	NC
18	HA21_P	User defined signal	NC	18	HA18_N	User defined signal	NC
20	HA21_N	User defined signal	NC	20	GND	GND	GND
21	GND	GND	GND	21	HA22_P	User defined signal	NC
22	HA23_P	User defined signal	NC	22	HA22_N	User defined signal	NC
23	HA23_N	User defined signal	NC	23	GND	GND	GND
24	GND	GND	GND	24	HB01_P	User defined signal	NC
25	HB00_P_CC	User defined signal	NC	25	HB01_N	User defined signal	NC
26	HB00_N_CC	User defined signal	NC	26	GND	GND	GND
27	GND	GND	GND	27	HB07_P	User defined signal	NC
28	HB06_P_CC	User defined signal	NC	28	HB07_N	User defined signal	NC
29	HB06_N_CC	User defined signal	NC	29	GND	GND	GND
30	GND	GND	GND	30	HB11_P	User defined signal	NC
31	HB10_P	User defined signal	NC	31	HB11_N	User defined signal	NC
32	HB10_N	User defined signal	NC	32	GND	GND	GND
33	GND	GND	GND	33	HB15_P	User defined signal	NC
34	HB14_P	User defined signal	NC	34	HB15_N	User defined signal	NC
35	HB14_N	User defined signal	NC	35	GND	GND	GND
36	GND	GND	GND	36	HB18_P	User defined signal	NC
37	HB17_P_CC	User defined signal	NC	37	HB18_N	User defined signal	NC
38	HB17_N_CC	User defined signal	NC	38	GND	GND	GND
39	GND	GND	GND	39	VIO_B_M2C	IO Bank Voltage	
40	VIO_B_M2C	IO Bank Voltage		40	GND		

Table (20): FMC Pin Assignment