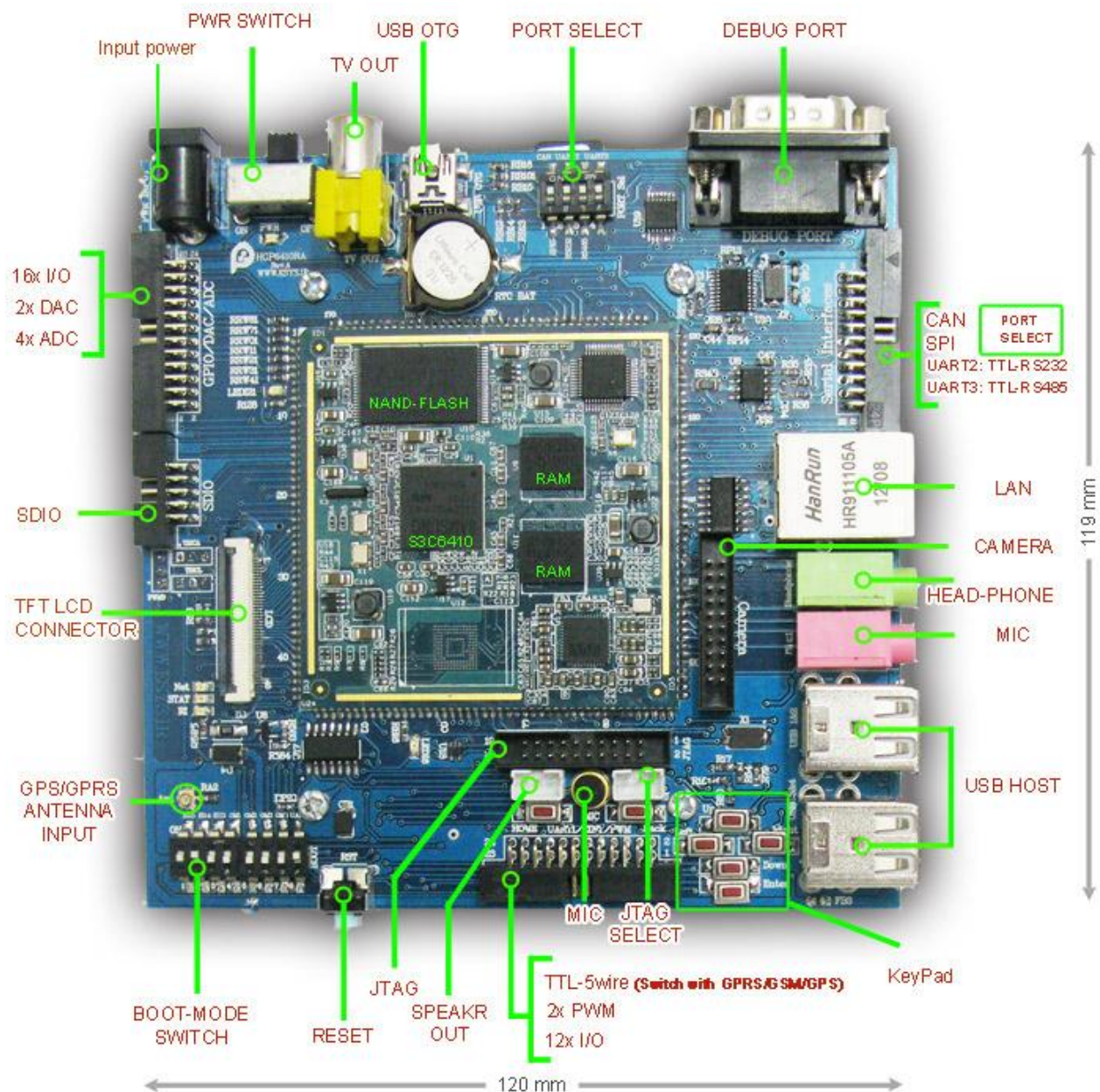




ILUM6410

راهنمای ویژگی های سخت افزاری و ظاهری







طراحی برد ILUM6410 بر اساس آی سی S3C6410 از شرکت سامسونگ است. در این آی سی از معماری ARM۱۱ و پردازنده ی ARM1176JZF-S استفاده شده است.

- بیشترین فرکانس کاری: 667MHz
- حافظه NAND Flash :1GB MLC
- حافظه mDDR :256MB

مشخصات و ویژگی های ILUM6410

- CPU
 - S3C6410 – ARM1176JZF-S frequency up to 667 MHz
- RAM
 - 256MB Onboard mDDR
- Nand Flash
 - 1GB MLC NAND Flash
- X1 RJ45 Ethernet Interface (100/10 Full Duplex)
- **X4 USB Host** Interface (Type-A, Supporting USB 1.1)
- **X37 GPIOs:**
 - X16 I/O
 - X12 External Interrupt
 - X7 SDIO CH0
 - X2 PWM



- Serial Interfaces
 - X1 UAR0_RS232(Debug Port)
 - X1 5-Wire UART1_TTL/(**GSM/GPRS/GPS Module**)
 - X1 UART2_TTL/**RS232**
 - X1 UART3_TTL/**RS485**
 - X1 SPI/**CAN v2.0B**
 - X1 I2C channel
- x1 40-pin FPC connector(**Supports 24bit TFT LCD**)
- Supports **4-Wire/1-Wire/I2C touch screen**
- Supports **GSM/GPRS/GPS module Onboard** (SIM908, SIM900, ...)
- Supports **VGA/AV Input/Camera/SDIO Wi-Fi and so on module**
- x1 **TV OUT(Composite)**
- **x2 DAC**
- x1 Audio Input Socket
- x1 Audio Output Socket
- x1 Speaker Output connector
- x1 **Microphone Onboard**
- x1 USB OTG (Supporting USB 2.0)
- X1 SD MMC/**Micro MMC** socket with detect pin
- X7 User Push Buttons
- X2 User LED
- On Board Real-time Clock
- X4 Channel ADC Input (10 bit)
- X1 20-pin JTAG Socket
- On Board EEPROM (I2C Protocol)



Pin Mapping:

Boot Modes (DIP-Switch):

PIN	1	2	3	4	5	6	7	8
	EINT15	EINT14	EINT13	OM1	OM2	OM3	OM4	GSM
<i>ON</i>	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	Connected to UART1
<i>OFF</i>	GND	GND	GND	GND	GND	GND	GND	Connected to GSM/GPS/GPRS

*Boot from SD MMC/Micro MMC: 1-7 must be off.

*Boot from Windows CE: 2 must be ON and 1, 3, 4, 5, 6, 7 must be OFF.

*Boot from Linux/Android: 1-5 must be OFF and 5, 6 must be ON.

Serial interfaces port selection (DIP-Switch):

PIN No.	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>
	CAN/SPI0	UART2_TTL/RS232	UART3_TTL/RS485	Idle
<i>ON</i>	CAN	UART2_TTL	UART3_TTL	-
<i>OFF</i>	SPI0	UART2_RS232	UART3_RS485	-

Serial interfaces pin mapping:

No.	Signal	Description	Detail	No.	Signal	Description	Detail
<u>1</u>	VDD5V	5V Power	Out	<u>2</u>	GND	Ground	-
<u>3</u>	Xi2cSCL/GPB5	IIC0_SCL	I2C	<u>4</u>	Xi2cSDA/GPB6	IIC0_SDA	I2C
<u>5</u>	CANL	Dominant Low	CAN	<u>6</u>	CANH	Dominant High	CAN
<u>7</u>	GND	Ground	-	<u>8</u>	SPI0_CS	Chip select	SPI
<u>9</u>	XspiMOSI0/GPC2	SPI0_MOSI	SPI	<u>10</u>	XspiCLK0/GPC1	SPI0_CLK	SPI
<u>11</u>	GND	Ground	-	<u>12</u>	XspiMISO0/GPC0	SPI0_MISO	SPI
<u>13</u>	RXD3B	Rx-UART3	TTL	<u>14</u>	TXD3B	Tx-UART3	TTL



<u>15</u>	RS485_P1	A-UART3	RS485	<u>16</u>	RS485_P2	B-UART3	RS485
<u>17</u>	VDD_IO	3.3V Power	Out	<u>18</u>	VDD_IO	3.3V Power	Out
<u>19</u>	GND	Ground	-	<u>20</u>	GND	Ground	-
<u>21</u>	RSRXD2	Rx-UART2	RS232	<u>22</u>	RSTXD2	Tx-UART2	RS232
<u>23</u>	RXD2B	Rx-UART2	TTL	<u>24</u>	TXD2B	Tx-UART2	TTL

Camera interface pin mapping:

No.	Signal	I/O	Description
<u>1</u>	Xi2cSDA/GPB6	I/O	IIC0_SDA
<u>2</u>	Xi2cSCL/GPB5	I/O	IIC0_SCL
<u>3</u>	-	-	NC
<u>4</u>	XciRSTn/GPF3	I/O	Reset
<u>5</u>	XciCLK/GPF0	I/O	Camera Clock Signal
<u>6</u>	XciHREF/GPF1	I/O	Camera Horizontal Sync
<u>7</u>	XciVSYNC/GPF4	I/O	Camera Vertical Sync
<u>8</u>	XciPCLK/GPF2	I/O	Camera Pixel Clock
<u>9</u>	XciYDATA7/GPF12	I/O	Camera Data Bit 7
<u>10</u>	XciYDATA6/GPF11	I/O	Camera Data Bit 6
<u>11</u>	XciYDATA5/GPF10	I/O	Camera Data Bit 5
<u>12</u>	XciYDATA4/GPF9	I/O	Camera Data Bit 4
<u>13</u>	XciYDATA3/GPF8	I/O	Camera Data Bit 3
<u>14</u>	XciYDATA2/GPF7	I/O	Camera Data Bit 2
<u>15</u>	XciYDATA1/GPF6	I/O	Camera Data Bit 1
<u>16</u>	XciYDATA0/GPF5	I/O	Camera Data Bit 0
<u>17</u>	VDD5V	PWR	5V
<u>18</u>	VDD_IO	PWR	3.3V
<u>19</u>	GND	PWR	Ground
<u>20</u>	GND	PWR	Ground

JTAG interface pin mapping:

No.	Signal	I/O	Description
<u>1</u>	VDD_IO	PWR	3.3V
<u>2</u>	VDD_IO	PWR	3.3V
<u>3</u>	XjTRST	I/O	JTAG RESET Signal
<u>4</u>	GND	PWR	Ground
<u>5</u>	XjTDI	I/O	JTAG TDI Signal
<u>6</u>	GND	PWR	Ground
<u>7</u>	XjTMS	I/O	JTAG TMS Signal
<u>8</u>	GND	PWR	Ground
<u>9</u>	XjTCK	I/O	JTAG TCK Signal
<u>10</u>	GND	PWR	Ground



<u>11</u>	XjRTCK	I/O	JTAG RTCK Signal
<u>12</u>	GND	PWR	Ground
<u>13</u>	XjTDO	I/O	JTAG TDO Signal
<u>14</u>	GND	PWR	Ground
<u>15</u>	XnRESET	I/O	JTAG RESET Signal
<u>16</u>	GND	PWR	Ground
<u>17</u>	-	-	NC
<u>18</u>	GND	PWR	Ground
<u>19</u>	-	-	NC
<u>20</u>	GND	PWR	Ground

JTAG select type:

No.	Signal	Description
<u>1</u>	GND	Ground
<u>2</u>	XDBGSEL	JTAG selection type: IF 1 : Peripherals JTAG, IF 0 : ARM1176JZF-S Core JTAG
<u>3</u>	DBGSEL_PU	Pull Up XDBGSEL

UART1/EINT/PWM interface pin mapping:

No.	Signal	I/O	Detail	No.	Signal	I/O	Detail
<u>1</u>	GND	PWR	Ground	<u>2</u>	VDD5V	PWR	5V
<u>3</u>	XpwmTOUT0/ XCLKOUT/GPF14	I/O	PWM Output 0	<u>4</u>	XpwmTOUT1/GPF15	I/O	PWM Output 1
<u>5</u>	GND	PWR	Ground	<u>6</u>	GND	PWR	Ground
<u>7</u>	XhiADDR10/IORD_C F/EINT18/GPL10	I/O	External Interrupt 18	<u>8</u>	XhiADDR12/IORDY_CF / EINT20/GPL12	I/O	External Interrupt 20
<u>9</u>	XhiADDR8/CE_CF0/ EINT16/GPL8	I/O	External Interrupt 16	<u>10</u>	XhiADDR9/CE_CF1/ EINT17/GPL9	I/O	External Interrupt 17
<u>11</u>	XEINT10/GPN10	I/O	External Interrupt 10	<u>12</u>	XEINT11/GPN11	I/O	External Interrupt 11
<u>13</u>	XEINT6/kpROW6/GP N6	I/O	External Interrupt 6	<u>14</u>	XEINT9/GPN9	I/O	External Interrupt 9



<u>15</u>	XEINT2/kpROW2/GP N2	I/O	External Interrupt 2	<u>16</u>	XEINT5/kpROW5/GPN5	I/O	External Interrupt 5
<u>17</u>	XEINT0/kpROW0/GP N0	I/O	External Interrupt 0	<u>18</u>	XEINT1/kpROW1/GPN1	I/O	External Interrupt 1
<u>19</u>	GND	PWR	Ground	<u>20</u>	VDD_IO	PWR	3.3V
<u>21</u>	XuRTSn1/GPA7	I/O	UART1 RTS_TTL	<u>22</u>	XuTXD1/GPA5	I/O	UART1 Tx_TTL
<u>23</u>	XuCTSn1/GPA6	I/O	UART1 CTS_TTL	<u>24</u>	XuRXD1/GPA4	I/O	UART1 Rx_TTL

****For using UART1, u must set 8th pin in boot modes DIP-Switch to ON.***

**** If 8th pin in boot modes DIP-Switch be OFF, means is connected to GSM/GPRS/GPS module.***

SPKR interface pin mapping:

No.	Signal	Description
<u>1</u>	GND_A	Analog Ground
<u>2</u>	SPKL	Audio Left Output
<u>3</u>	SPKR	Audio Right Output

LCD En (Enable) interface pin mapping:

No.	Signal	Detail	Description
<u>1</u>	XpwmTOUT0/ XCLKOUT/GPF14	PWM Output 0	Connect to PWM in case of using 4-wire Touch-Screen (If your OS can control Back-Light through this Pin)
<u>2</u>	PWM	-	Back-Light Enable
<u>3</u>	PWM_M	-	Connect to PWM in case of using 4-wire Touch-Screen (For Permanent ON Back-Light)

PU_I2C interface pin mapping:

No.	Signal	Description
<u>1</u>	VDD_IO	Connect to VDD_IO/I2C in case of NOT using I2C Touch-Screen
<u>2</u>	VDD_IO/I2C	
<u>3</u>	Xi2cSCL/GPB5	Connect to VDD_IO/I2C in case of using I2C Touch-Screen

***1W_I2C interface pin mapping:***

No.	Signal	Description
<u>1</u>	XpwmTOUT1/GPF15	Connect to PWM in case of using 1-wire Touch-Screen
<u>2</u>	PWM/I2C	
<u>3</u>	Xi2cSDA/GPB6	Connect to VDD_IO/I2C in case of using I2C Touch-Screen

SDIO interface pin mapping:

No.	Signal	I/O	Detail	No.	Signal	I/O	Detail
<u>1</u>	VDD_IO	PWR	3.3V	<u>2</u>	VDD5V	PWR	5V
<u>3</u>	GND	PWR	Ground	<u>4</u>	XmmcCMD0/ GPG1	I/O	SDIO 0 command signal Pull-up resistor 10k
<u>5</u>	XmmcDATA0_3 /GPG5	I/O	SDIO 0 data bit 3 Pull-up resistor 10k	<u>6</u>	XmmcCLK0/ GPG0	I/O	SDIO 0 output clock Pull-up resistor 10k
<u>7</u>	XmmcDATA0_1/GPG3	I/O	SDIO 0 data bit 1 Pull-up resistor 10k	<u>8</u>	XmmcDATA0_2/GPG4	I/O	SDIO 0 data bit 2 Pull-up resistor 10k
<u>9</u>	XEINT12/ GPN12	I/O	SDIO 0 Chip select, low enable Pull-up resistor 10k	<u>10</u>	XmmcDATA0_0/GPG2	I/O	SDIO 0 data bit 0 Pull-up resistor 10k

***GPIO/DAC/ADC interface pin mapping:***

No.	Signal	I/O	Detail	No.	Signal	I/O	Detail
<u>1</u>	XhiDATA8/kpROW0/ CF_DATA8/GPK8	I/O	Keypad row 0	<u>2</u>	XhiDATA9/kpROW1/ CF_DATA9/GPK9	I/O	Keypad row 1
<u>3</u>	XhiDATA10/kpROW2/ CF_DATA10/GPK10	I/O	Keypad row 2	<u>4</u>	XhiDATA11/kpROW3/ CF_DATA11/GPK11	I/O	Keypad row 3
<u>5</u>	XhiDATA12/kpROW4/ CF_DATA12/GPK12	I/O	Keypad row 4	<u>6</u>	XhiDATA13/kpROW5/ CF_DATA13/GPK13	I/O	Keypad row 5
<u>7</u>	XhiDATA14/kpROW6/ CF_DATA14/GPK14	I/O	Keypad row 6	<u>8</u>	XhiDATA15/kpROW7/ CF_DATA15/GPK15	I/O	Keypad row 7
<u>9</u>	XhiADDR7/kpCOL7/ Xm0CData/GPL7	I/O	Keypad column 7	<u>10</u>	XhiADDR6/kpCOL6/ Xm0REGata/GPL6	I/O	Keypad column 6
<u>11</u>	XhiADDR5/kpCOL5/ Xm0INPACKata/GPL5	I/O	Keypad column 5	<u>12</u>	XhiADDR0/kpCOL0/ CF_ADDR0/GPL0	I/O	Keypad column 0
<u>13</u>	XhiADDR4/kpCOL4/ Xm0RSTata/GPL4	I/O	Keypad column 4	<u>14</u>	XhiADDR3/kpCOL3/ Xm0INTata/GPL3	I/O	Keypad column 3
<u>15</u>	XhiADDR2/kpCOL2/ CF_ADDR2/GPL2	I/O	Keypad column 2	<u>16</u>	XhiADDR1/kpCOL1/ CF_ADDR1/GPL1	I/O	Keypad column 1
<u>17</u>	VDD_IO	PWR	3.3V	<u>18</u>	GND	PWR	Ground
<u>19</u>	XdacOUT_1	-	TV out 1	<u>20</u>	XdacOUT_0	-	TV out 0
<u>21</u>	Xadc_AIN2	-	ADC channel 2	<u>22</u>	Xadc_AIN3	-	ADC channel 3
<u>23</u>	Xadc_AIN1	-	ADC channel 1	<u>24</u>	Xadc_AIN0	-	ADC channel 0

Important Notes:

In case of using GPS Active antenna, for 2.8 V power supply use 0 Ohm resistor instead of RAct and for 3.3 V power supply utilize 0 Ohm resistor in the place of RAct2. Never put these two resistors in circuit at the same time.

To facilitate the antenna tuning, an antenna matching circuit should be added. In this board, the components RA, RA2, CA1, and CA2 are used for antenna matching.



بلوک دیاگرام



در این برد به طور کلی 37 پین GPIO وجود دارد که بر اساس سیستم عامل پیش ساخته فقط 28 پین آزاد به عنوان GPIO معرفی شده اند و بقیه پین ها به توابع دیگری اختصاص داده شده است. اما تمام این پین ها می توانند با سفارشی کردن سیستم عامل، به عنوان GPIO مورد استفاده قرار گیرند.



مشخصات مکانیکال

